

## PLL lock detector

### SPECIFICATION

#### 1 FEATURES

- TSMC018 SiGe 0.18 $\mu$ m
- Low current consumption
- High accuracy
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SiTerra

#### 2 APPLICATION

- Phase-locked loop synthesizer

#### 3 OVERVIEW

The lock detector monitors the current status of PLL by comparing the phase difference of VCO divided signal and reference oscillator signal with required value. SelTime<1:0> and SelErr outputs set the lock monitoring period and the lock detector accuracy, respectively. The block is fabricated on TSMC018 SiGe 0.18 $\mu$ m technology.

#### 4 STRUCTURE

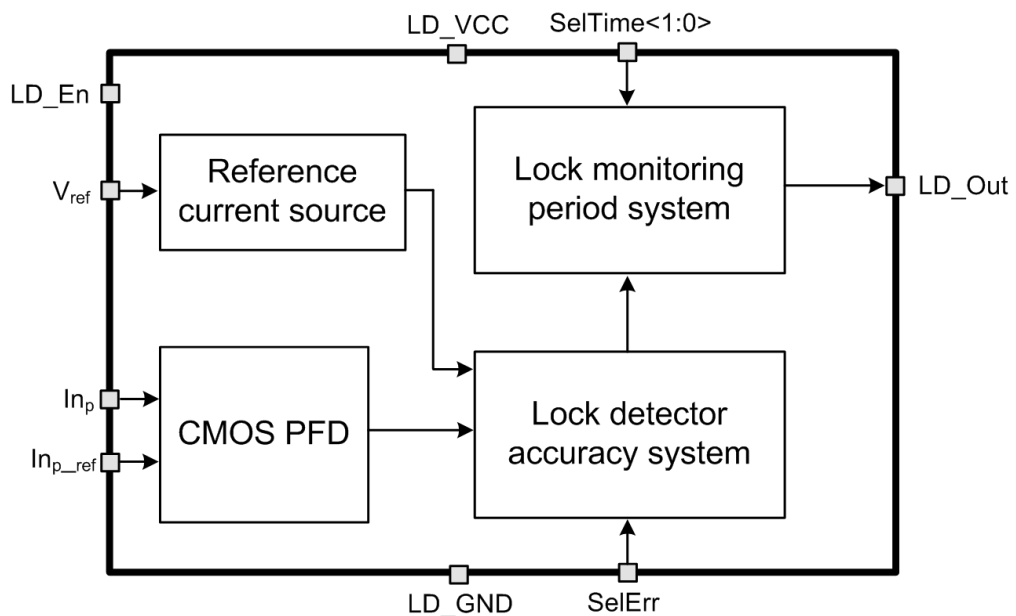


Figure 1: PLL lock detector structure.

## 5 PIN DESCRIPTION

Name	Direction	Description
V <sub>ref</sub>	IO	Reference voltage
IN_p	I	Input of VCO divided signal
IN_p_ref	I	Input of reference oscillator signal
SelTime<1:0>	I	Lock monitoring period
SelErr	I	Lock detector accuracy
LD_OUT	O	Lock indicator output
LD_En	I	Enable/disable lock detector
LD_VCC	IO	Supply voltage
LD_GND	IO	Ground

## 6 LAYOUT DESCRIPTION

PLL lock detector dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	67	$\mu\text{m}$
Width	122	$\mu\text{m}$

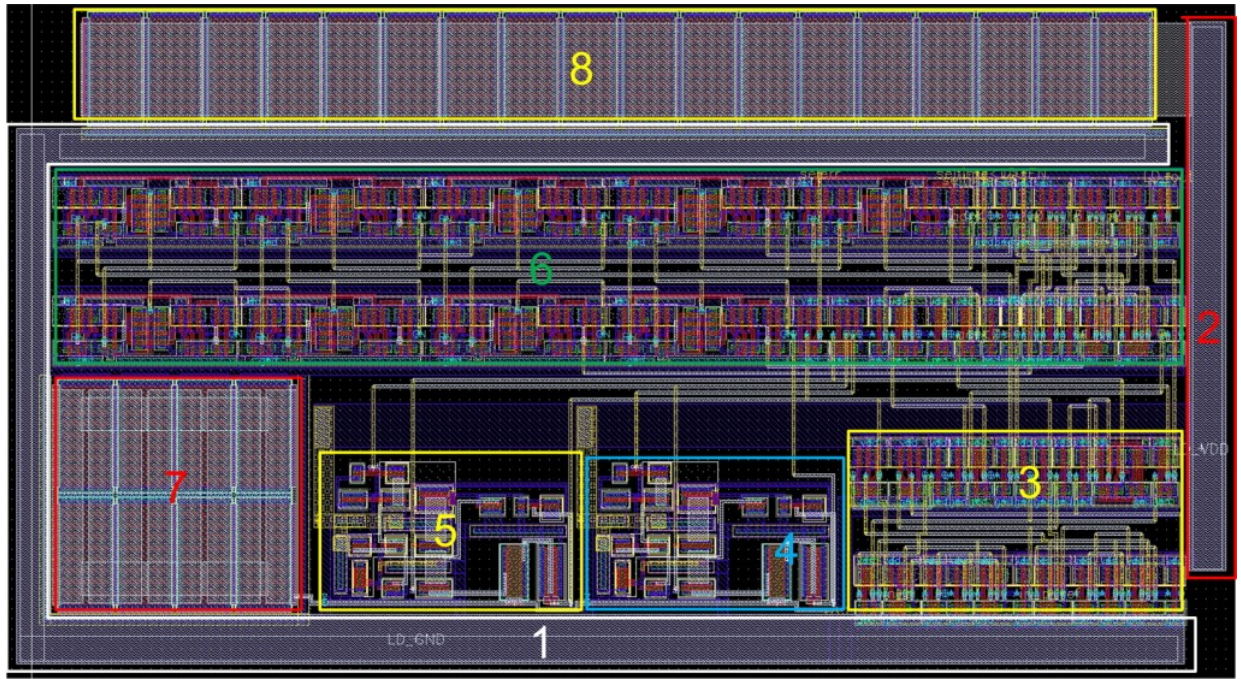


Figure 2: PLL lock detector layout view.

1. Ground bus
2. Supply voltage bus
3. CMOS PFD
- 4,5. Lock detector accuracy system
6. Lock monitoring period system
7. Reference current source with filters
8. Supply voltage bus filter

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ TSMC018 SiGe  
 Status \_\_\_\_\_ silicon proven  
 Area \_\_\_\_\_ 0.009 mm<sup>2</sup>

### 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{cc} = 2.8 \div 3.6$  V и  $T = -40 \div +85^{\circ}\text{C}$ . Typical values are at  $V_{cc} = 3.15$  V,  $T = +27^{\circ}\text{C}$ , unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	$V_{cc}$	-	2.8	3.15	3.6	V
Operating temperature range	T	-	-40	+27	+85	°C
Peak-to-peak input voltage	$A_{in\ p-p}$	For inputs IN_p, IN_p_ref	$V_{cc} - 0.4$	$V_{cc}$	$V_{cc} + 2.4$	V
Lock monitoring period*	MP	$T_{ref} = \frac{1}{F_{ref}}$	$64 \times T_{ref}$	-	$512 \times T_{ref}$	μs
Lock detector accuracy	ACR	SelErr** = "0"	5.5	6	7	ns
		SelErr** = "1"	10	12	13	
Supply current	$I_{cc}$	-	45	90	115	μA
Stand-by current	$I_{stb}$	-	20	25	30	nA
Input logic-level high	$V_{IH}$	For digital inputs	$0.7 V_{cc}$	-	$V_{cc} + 0.25$	V
Input logic-level low	$V_{IL}$		-0.25	-	0.3	V

Note:

\* –  $F_{ref}$  – reference frequency.

\*\* – SelErr – digital code setting the lock detector accuracy.

## 8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation