PLL lock detector

SPECIFICATION

1 FEATURES

- AMS035 BiCMOS
- Low current consumption
- High accuracy
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

2 APPLICATION

- Phase-locked loop synthesizer

3 OVERVIEW

The lock detector monitors the current status of PLL by comparing the phase difference of VCO divided signal and reference oscillator signal with required value. SelTime<1:0> and SelErr outputs set the lock monitoring period and the lock detector accuracy, respectively.
The block is fabricated on AMS035 BiCMOS 0.35µm technology.

4 STRUCTURE

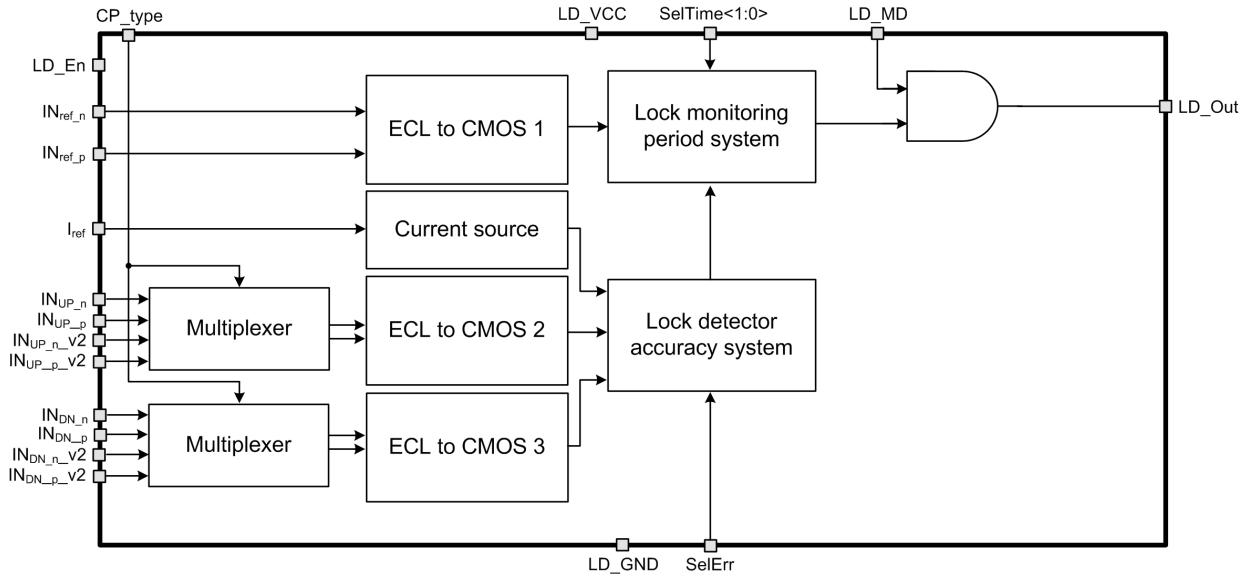

Figure 1: PLL lock detector structure.

5 PIN DESCRIPTION

Name	Direction	Description
I_{ref}	IO	Reference current
IN_{UP_n}	I	Differential input of PFD signal defined by the positive phase difference of VCO divided signal and reference oscillator signal
IN_{UP_p}	I	
IN_{DN_n}	I	Differential input of PFD signal defined by the negative phase difference of VCO divided signal and reference oscillator signal
IN_{DN_p}	I	
IN_{UP_n}	I	Differential input of the second PFD signal defined by the positive phase difference of VCO divided signal and reference oscillator signal
IN_{UP_p}	I	
IN_{DN_n}	I	Differential input of the second PFD signal defined by the negative phase difference of VCO divided signal and reference oscillator signal
IN_{DN_p}	I	
IN_{ref_n}	I	Differential input of reference oscillator signal
IN_{ref_p}		
SelTime<1:0>	I	Lock monitoring period
SelErr	I	Lock detector accuracy
CP_type	I	Charge pump input type: the first or the second
LD_MD	I	Lock detector mode selection: single or continuous tracking
LD_OUT	O	Lock indicator output
LD_En	I	Enable/disable lock detector
LD_VCC	IO	Supply voltage
LD_GND	IO	Ground

6 LAYOUT DESCRIPTION

PLL lock detector dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	225	µm
Width	130	µm

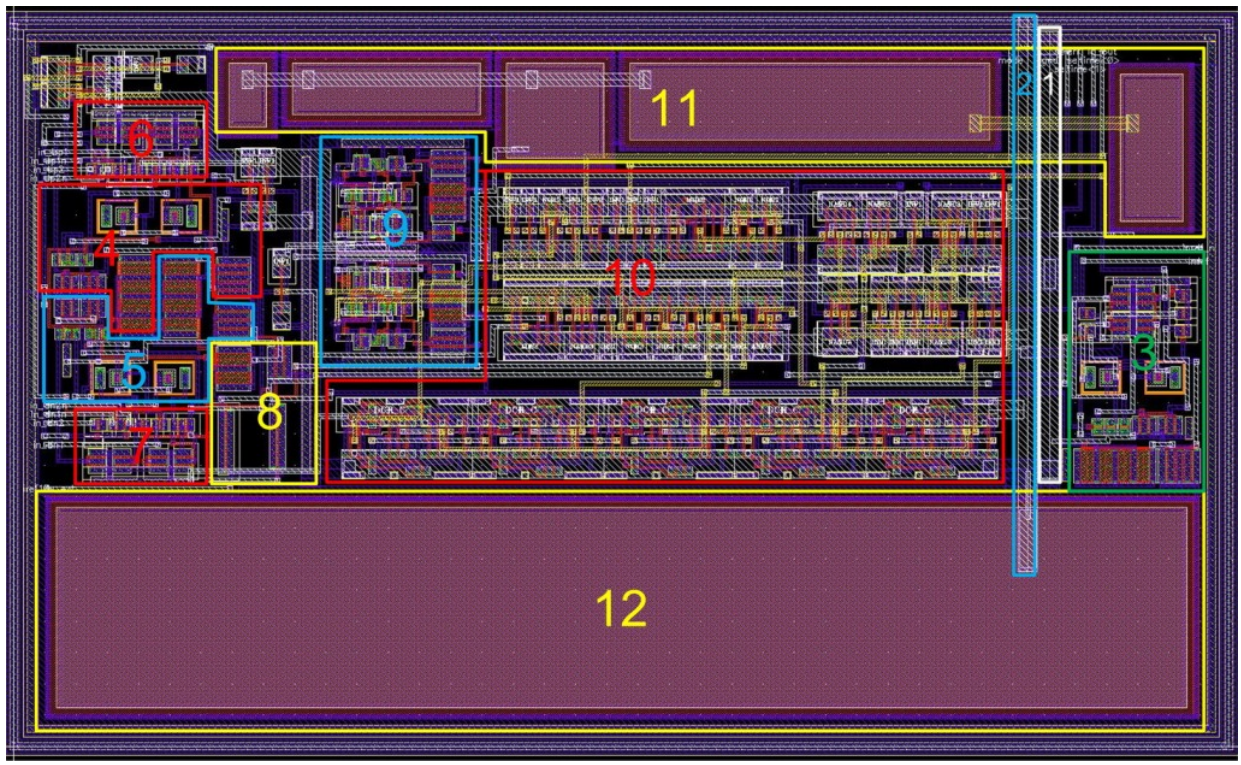

Figure 2: PLL lock detector layout view.

1. Ground bus
2. Supply voltage bus
3. ECL to CMOS 1
4. ECL to CMOS 2
5. ECL to CMOS 3
6. Multiplexer 1
7. Multiplexer 2
8. Reference current source
9. Lock detector accuracy system
10. Lock monitoring period system
11. Reference voltage filter
12. Supply voltage bus filter

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology AMS035 BiCMOS
Status silicon proven
Area 0.03 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.85 ÷ 3.15 V и T = -40 ÷ +85 °C. Typical values are at V_{cc} = 3.15 V, T = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	2.85	3.0	3.15	V
Operating temperature range	T	-	-40	+27	+85	°C
Peak-to-peak differential input voltage	$A_{in\ p\text{-}p}$	For inputs IN_{UP_n}, IN_{UP_p}, IN_{DN_n}, IN_{DN_p}, IN_{UP_n}_v2, IN_{UP_p}_v2, IN_{DN_n}_v2, $IN_{DN\ p}$_v2	0.4	-	1.6	V
DC operating point	V_{op}	-	V_{cc} - 1.4	-	V_{cc} - 0.6	V
Lock monitoring period*	MP	$T_{ref} = \frac{1}{F_{ref}}$	32×T_{ref}	-	256×T_{ref}	µs
Lock detector accuracy	ACR	SelErr** = "0"	7.0	8.5	10.5	ns
		SelErr** = "1"	14.0	16.5	20.5	
Supply current	I_{cc}	-	110	120	145	µA
Stand-by current	I_{stb}	-	0.4	0.5	122	nA
Input logic-high level	V_{IH}	For digital inputs LD_En, Seltime<1:0>	0.7 V_{cc}	-	V_{cc} +0.25	V
Input logic-low level	V_{IL}		-0.25	-	0.3	V

Note:
*– F_{ref} – reference frequency.
** – SelErr – digital code setting the lock detector accuracy.

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation