

30 mA LDO voltage regulator (output voltage 0.9 V ... 1.3 V)

SPECIFICATION

1 FEATURES

- Global Foundries CMOS 55 nm
- Low drop out
- Low current consumption
- Two modes operations: “Normal”, “Economy”
- No discrete filtering capacitors required (cap-less solution)
- Output voltage trimming 0.9 V ... 1.3 V
- Small area
- Can be ported to foundries TSMC, UMC, SMIC, iHP, AMS, Vanguard, SilTerra and other also compatible to with different technology nodes¹

2 APPLICATION

- Supply voltage sensitive circuits

3 OVERVIEW

The voltage regulator is used to maintain a stable output voltage at varying input voltage. The block consists of a differential amplifier, pass transistor and resistor's divider. Differential amplifier compares reference voltage with voltage from a feedback divider and adjusts the impedance of a PMOS transistor for stabilization of output voltage at required level. The output voltage adjustment is defined by the trimming code `trim<5:0>`. The block has low current consumption and allows high current load.

The block is designed on Global Foundries CMOS 55 nm technology.

¹ For more information contact NTLab

4 FUNCTIONAL DESCRIPTION

For best results, the block must be used together with IP 055GF_BVR_01, using its output signals.

4.1 PINS FOR ENABLING AND DISABLING BLOCK

Input signal **en** should be set to logical “1” or logical “0”. The high level of the signal turns on block and a low level signal disables it. Behavior of output signal during switching on and off block is shown at **Figure 1**.

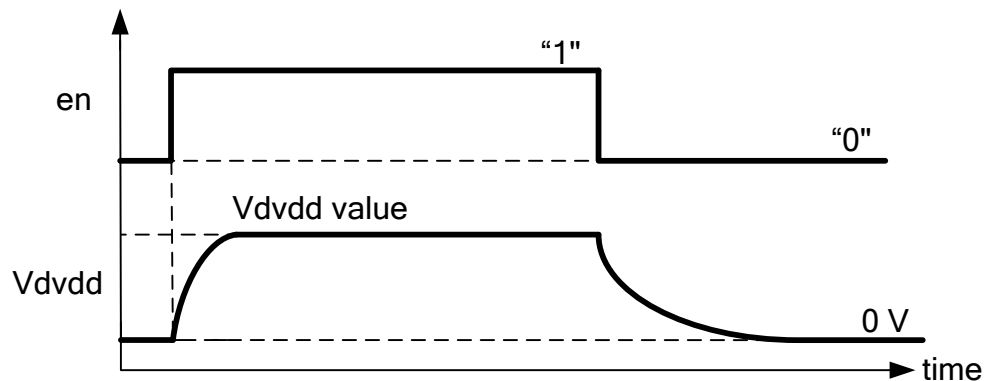


Figure 1: Timing diagram of switching on and off signal **dvdd**

4.2 PINS FOR TRIMMING THE OUTPUT VOLTAGE

Dependence of the output voltage **dvdd** from trimming code is shown at **Figure 2**. The output voltage **dvdd** increases linearly with the code (see the table in section 6).

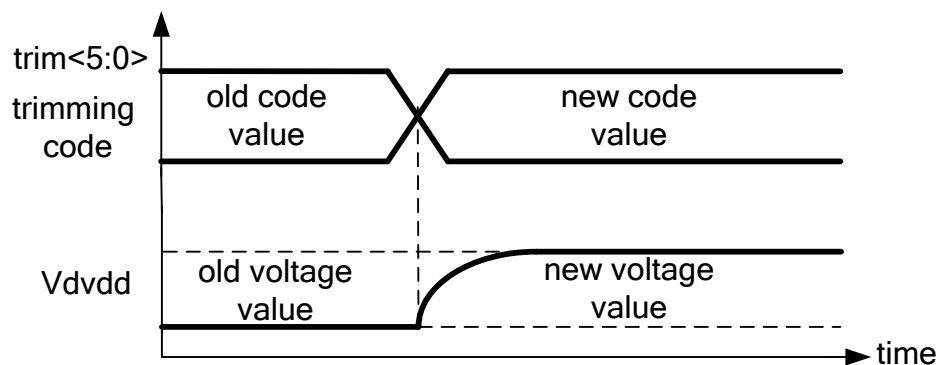


Figure 2: Timing diagram output voltage **dvdd** vs trimming code

4.3 PINS FOR OUTPUT SIGNALS

Pin for output signal is LDO voltage regulator output pin **dvdd**. Output pin **dvdd** assumes a capacitive load up to 20 nF and DC load in two modes: “Normal” from 0 to 30 mA and “Economy” from 0 to 2 mA. The load is connected between the output and ground. By increasing the load capacitance will increase the settling time. If exceed the current load, the correct voltage is not guaranteed.

4.4 OPERATION MODES

The LDO can operate in two modes: “Normal” and “Economy”. “Economy” mode is introduced to save battery power. Although the mode may handle full current load, it has slower reactions on load current change. “Normal” mode is a default LDO mode with minimum response time on load change.

5 STRUCTURE

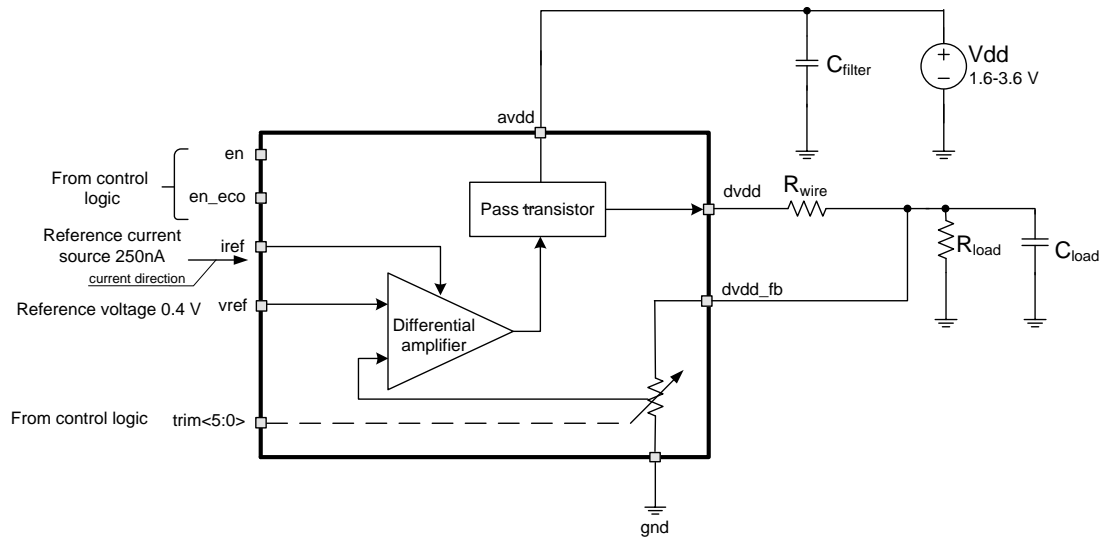


Figure 3: LDO voltage regulator structure and application diagram

6 PIN DESCRIPTION

Name	Direction	Description
en	I	LDO enable: “0” disabled “1” enabled
en_eco	I	LDO mode: “0” normal “1” economy
trim<5:0>	I	LDO trimming value: “000000” 0.85 V ... ~ step 7.96 mV “000110” 0.89 V ... ~ step 7.96 mV “010011” 1 V ... ~ step 7.96 mV “100000” 1.1 V ... ~ step 7.96 mV “101100” 1.2 V ... ~ step 7.96 mV “111000” 1.3 V ... ~ step 7.96 mV “111111” 1.35 V
vref	I	Reference voltage 0.4 V
iref	IO	Reference current 250 nA
dvdd	IO	LDO output
dvdd_fb	IO	LDO output voltage feedback. For best results, this pin necessary to connect close to the center of the domain in order to compensate a voltage drop on transmission line
avdd	IO	Analog supply voltage
gnd	IO	Ground

Note: * I – input, O – output

7 LAYOUT DESCRIPTION

7.1 TECHNOLOGY OPTIONS

LDO voltage regulator is designed under Global Foundries CMOS 55 nm technology process with following options:

- 4_02_00_00_LB option
- 2 metal levels of 1x (thin) width are used for routing
- High-Vt NFET and PFET
- Thick-oxide native (DG) NFET
- Thick-oxide I/O NFET and PFET (3.3V)
- P+ polysilicon OP resistor
- N+ diffusion OP resistor
- APMOM capacitor

7.2 PHYSICAL DIMENTIONS

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	102	um
Width	263	um

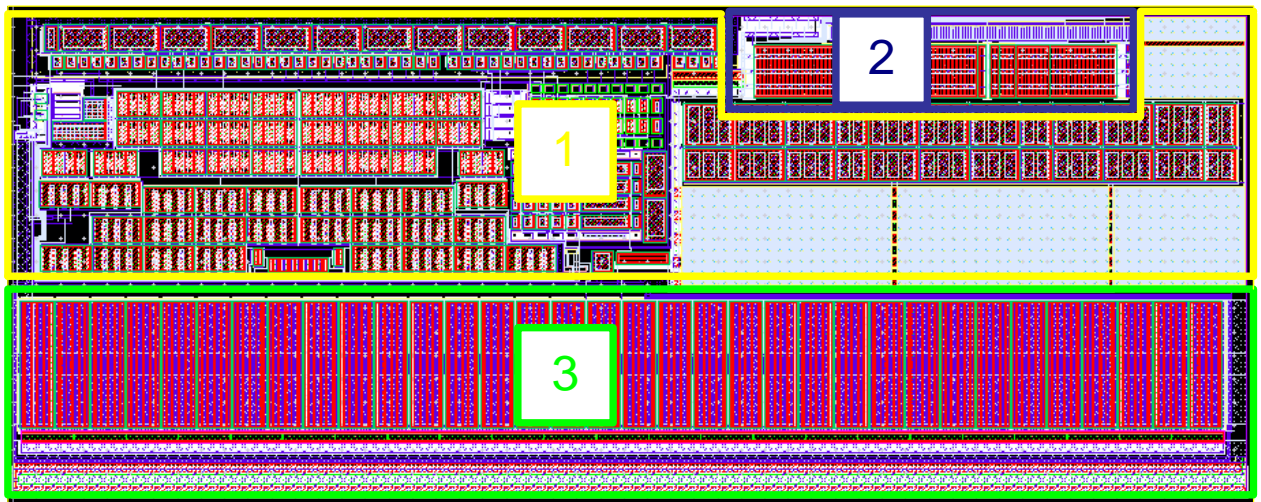


Figure 4: LDO voltage regulator layout

1. Amplifier
2. Trimming structure
3. Pass transistor

8 INTEGRATION GUIDELINES

8.1 INPUT SIGNALS

Signals `en`, `en_eco`, `trim<5:0>` are digital input signals, therefore not subject to special requirements.

Capacitance of pin `en` is 8.1 fF.

Capacitance of pin `en_eco` is 5 fF.

Capacitances of pins `trim <5:0>` is 3.5 fF.

8.2 PLACEMENT AND ROUTING

The following recommendations are given:

1. LDO voltage regulator layout can be rotated and flipped in axis X and Y
2. Pin `dvdd` connection to blocks being fed: series resistance should not exceed 0.5 Ohm, maximum current is 30 mA
3. For best results, pin `dvdd_fb` (feedback) can be connected with `dvdd` in the point of voltage regulation. Series resistance of the interconnect should be less than 1 kOhm
4. Ground (pin `gnd`) wire should allow flowing of 50 uA DC, 0.5 mA peak currents and should have resistance of less than 10 Ohm between pins and pads
5. Power supply (pin `avdd`) wire should allow flowing of 30 mA DC, 150 mA peak currents and should have resistance of less than 0.05 Ohm between pins and pads
6. External capacitance (not more than 20 nF) and internal capacitance should be connected to pin `avdd` for additional noise filtering. Internal capacitance should be added as much as possible
7. Is necessary to avoid parasitic capacitance coupling to the wire between reference current source and pin `iref` and wires, which have digital signals, as this can lead to a stable output pulsations voltage. If there is a need to conduct the connecting wires over the wire between reference current source and pin `iref`, it is necessary to apply the metal shielding of the wire. Shielding metal should be connected to the ground
8. No routing is allowed over the block in layers M1—M2

Other pins, not described here, have no special routing guidelines.

8.3 LAYOUT VERIFICATION

- DRC and LVS are run using Mentor Graphics Calibre
- No dummy structures are required for layers PC, RX, M1—M2

9 OPERATION CHARACTERISTICS

9.1 TECHNICAL CHARACTERISTICS

Technology _____ Global Foundries CMOS 55 nm
 Status _____ silicon proven
 Area _____ 0.027 mm²

9.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{avdd} = 1.6 \div 3.6$ V, $V_{ref} = 0.4$ V, $I_{ref} = 250$ nA and $T_j = -40 \div +85$ °C. Typical values are at $V_{avdd} = 2.5$ V and $T_j = 27$ °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{avdd}	-	1.6	2.5	3.6	V
Operating temperature range	T_j	-	-40	27	+85	°C
Minimum output voltage	V_{dvdd_min}	-	-	-	0.9	V
Maximum output voltage	V_{dvdd_max}	-	1.3	-	-	
Load capacitance	C_{load}	-	-	0.5	20	nF
Max load current	I_{load}	Normal mode	30	-	-	mA
		Economy mode	2	-	-	
Current consumption	I_{cc}	Normal mode	-	15	-	uA
		Economy mode	-	3	-	
Input logic-level low	V_{IL}	For digital signals	0	-	$0.3 \cdot V_{avdd}$	V
Input logic-level high	V_{IH}		$0.7 \cdot V_{avdd}$	-	V_{avdd}	

10 TYPICAL CHARACTERISTICS

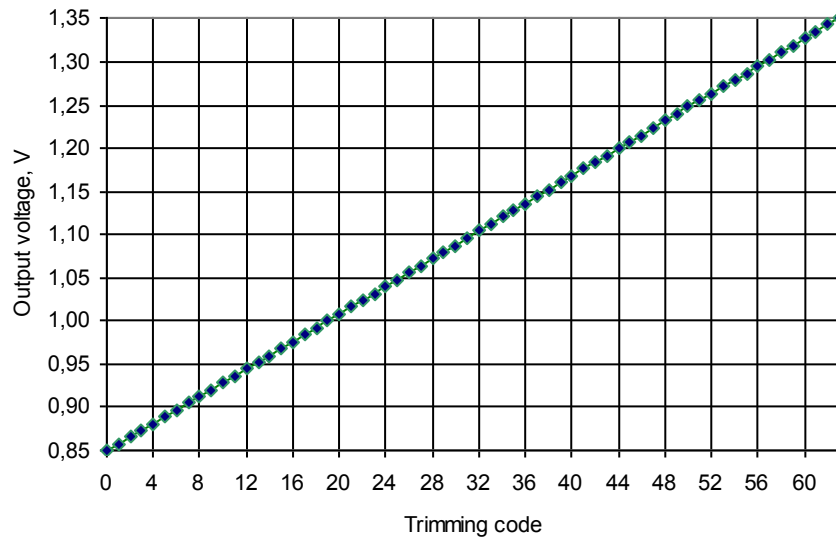


Figure 5: LDO output voltage vs trimming code

11 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

12 REVISION HISTORY

From version 1.0:

- Section 1 “Features” updated
- Section 3 “Overview” updated
- Section 4 “Structure” shifted to section 5
- Section 4 “Functional description” updated
- Section 5 “Structure”. Figure 3 updated
- Section 6 “Pin description” updated
- Subsection 7.1 “Technology options” updated
- Subsection 7.2 “Physical dimensions”. Figure 4 updated
- Section 8 “Integration guidelines” updated
- Section 9 “Operation characteristics” updated
- Section 10 “Typical characteristics”. Figure 5 updated
- Section 11 “Deliverables” updated