30 mA flash LDO voltage regulator (output voltage 1.8 ± 0.2 V)

SPECIFICATION

1 FEATURES

- Global Foundries CMOS 55 nm
- Low drop out
- Low current consumption
- Two modes operations: “Normal”, “Economy”
- Mode operation “Bypass”
- No discrete filtering capacitors required (cap-less solution)
- Output voltage trimming 1.8 V ± 0.2 V
- Small area
- Can be ported to foundries TSMC, UMC, SMIC, iHP, AMS, Vanguard, SilTerra and other also compatible to with different technology nodes[1]

2 APPLICATION

- Supply voltage sensitive circuits

3 OVERVIEW

The voltage regulator is used to maintain a stable output voltage at varying input voltage. The voltage regulator consists of a differential amplifier, pass transistor and resistor's divider. Differential amplifier compares reference voltage with voltage from a feedback divider and adjusts the impedance of a PMOS transistor for stabilization of output voltage at a set level. The output voltage adjustment is defined by the trimming code trim<5:0>. The block has low supply current and allows high current load.
The block is designed on Global Foundries CMOS 55 nm technology.

[1] For more information contact NTLab

4 FUNCTIONAL DESCRIPTION

For best results, the block must be used together with IP 055GF_BVR_01, using its output signals.

4.1 PINS FOR ENABLING AND DISABLING BLOCK

Input signal en should be set to logical “1” or logical “0”. The high level of the signal turns on block and a low level signal disables it. Behavior of output signal during switching on and off block is shown at Figure 1.

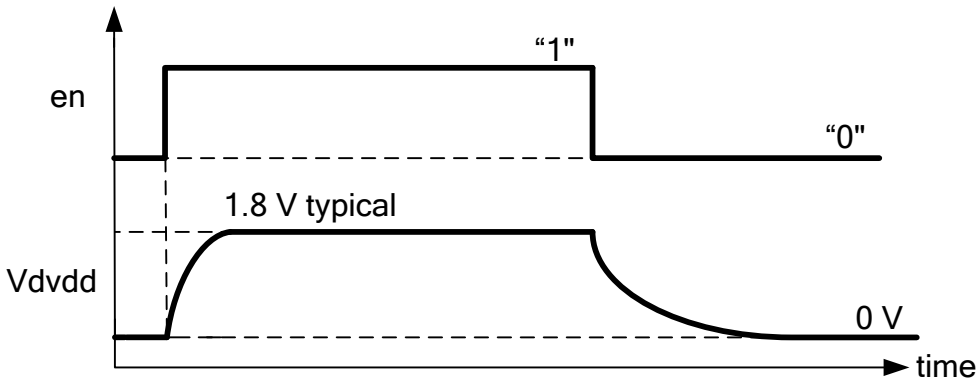

Figure 1: Timing diagram of switching on and off signal dvdd

4.2 PINS FOR TRIMMING THE OUTPUT VOLTAGE

Dependence of the output voltage dvdd from trimming code is shown at Figure 2. The output voltage dvdd increases linearly with the code (see the table in section 6).

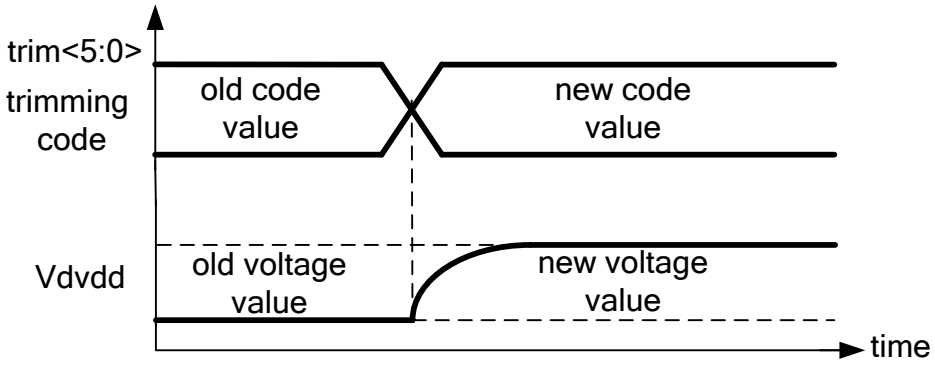

Figure 2: Timing diagram output voltage dvdd vs trimming code

4.3 PINS FOR OUTPUT SIGNALS

Pin for output signal is LDO voltage regulator output pin dvdd. Output pin dvdd assumes a capacitive load typical 0.5 nF and DC load in two modes: “Normal” from 0 to 30 mA and “Economy” from 0 to 3 mA. The load is connected between the output and ground. By increasing the load capacitance will increase the settling time. If exceed the current load, the correct voltage is not guaranteed.

4.4 OPERATION MODES

The LDO can operate in two modes: “Normal” and “Economy”. “Economy” mode is introduced to save battery power. Although the mode may handle full current load, it has slower reactions on load current change. “Normal” mode is a default LDO mode with minimum response time on load change.

"Bypass" mode is a LDO mode of the pass transistor with minimum channel resistance, independently of the output signal of the differential amplifier.

5 STRUCTURE

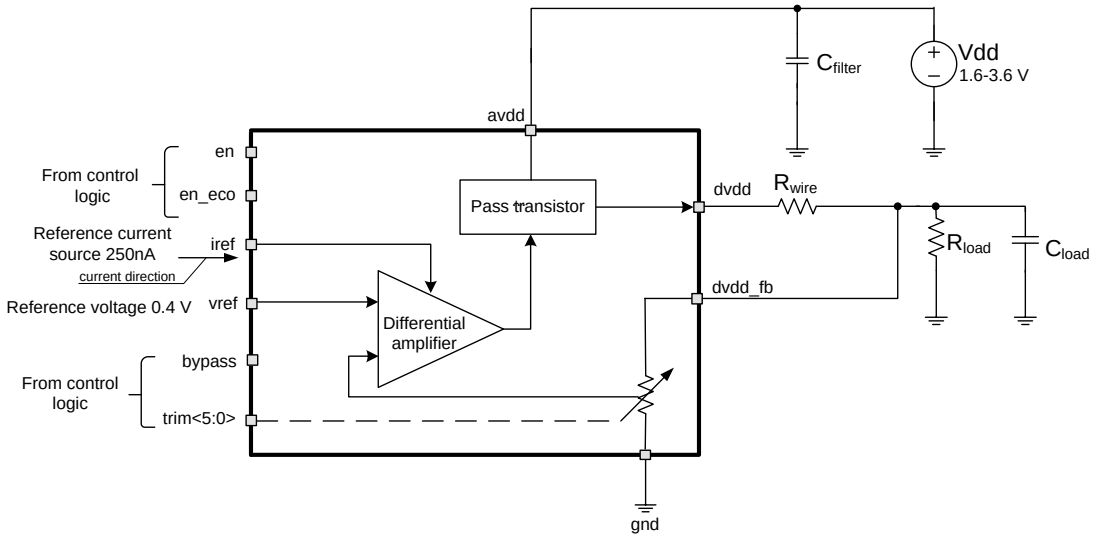

Figure 3: Flash LDO voltage regulator structure and application diagram

6 PIN DESCRIPTION

Name	Direction	Description
en	I	LDO enable: “0” disabled “1” enabled
en_eco	I	LDO mode: “0” normal “1” economy
trim<5:0>	I	LDO trimming value: “000000” 1.554 V … ~ step 7.99 mV “100000” 1.81 V … ~ step 7.99 mV “111111” 2.057 V
iref	IO	Reference current 250 nA
vref	I	Reference voltage 0.4 V
bypass	I	LDO bypass mode: “0” output voltage regulation “1” bypass
dvdd	IO	LDO output
dvdd_fb	IO	LDO output voltage feedback. For best results, this pin necessary to connect close to the center of the domain in order to compensate a voltage drop on transmission line
avdd	IO	Analog supply voltage
gnd	IO	Ground

Note: * I – input, O – output

7 LAYOUT DESCRIPTION

7.1 TECHNOLOGY OPTIONS

Flash LDO voltage regulator is designed under Global Foundries CMOS 55 nm technology process with following options:

- 4_02_00_00_LB option
- 2 metal levels of 1x (thin) width are used for routing
- Thick-oxide native (DG) NFET
- Thick-oxide I/O NFET and PFET (3.3 V)
- P+ polysilicon OP resistor
- N+ diffusion OP resistor
- APMOM capacitor

7.2 PHYSICAL DIMENTIONS

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	100	um
Width	293	um

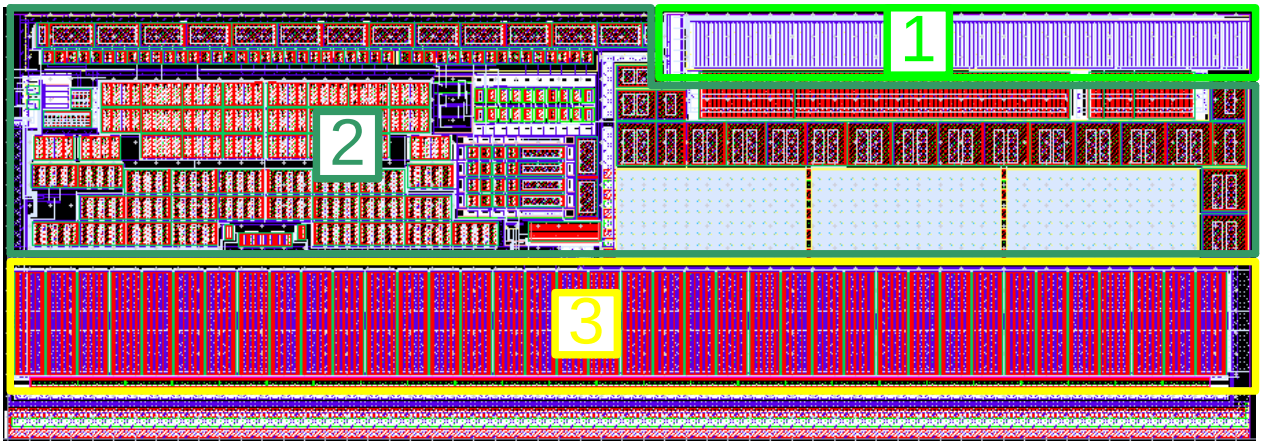

Figure 4: Flash LDO voltage regulator layout

1. Trimming structure
2. Amplifier
3. Pass transistor

8 INTEGRATION GUIDELINES

8.1 INPUT AND OUTPUT SIGNALS

Signals en, en_eco, bypass, trim<5:0> are digital input signals, therefore not subject to special requirements.
Capacitance of pin en is 8 fF.
Capacitance of pin en_eco is 4.5 fF.
Capacitance of pin bypass is 9 fF.
Capacitances of pins trim<5:0> is 4.5 fF.

8.2 PLACEMENT AND ROUTING

The following recommendations are given:

1. Flash LDO voltage regulator layout can be rotated and flipped in axis X and Y
2. Pin dvdd connection to blocks being fed: series resistance should not exceed 0.5 Ohm, maximum current is 30 mA
3. For best results, pin dvdd_fb (feedback) can be connected with pin dvdd in the point of voltage regulation. Series resistance of the interconnect should be less than 1 kOhm
4. Ground (pin gnd) wire should allow flowing of 50 uA DC, 0.5 mA peak currents and should have resistance of less than 10 Ohm between pins and pads
5. Power supply (pin avdd) wire should allow flowing of 30 mA DC, 150 mA peak currents and should have resistance of less than 0.05 Ohm between pins and pads
6. External capacitance (typical 0.5 nF) and internal capacitance should be connected to pin avdd for additional noise filtering. Internal capacitance should be added as much as possible
7. Is necessary to avoid parasitic capacitance coupling to the wire between reference current source and pin iref and wires, which have digital signals, as this can lead to a stable output pulsations voltage. If there is a need to conduct the connecting wires over the wire between reference current source and pin iref, it is necessary to apply the metal shielding of the wire. Shielding metal should be connected to the ground
8. No routing is allowed over the block in layers M1—M2

Other pins, not described here, have no special routing guidelines.

9 OPERATION CHARACTERISTICS

9.1 TECHNICAL CHARACTERISTICS

Technology Global Foundries CMOS 55 nm
Status silicon proven
Area 0.029 mm^2

9.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{avdd} = 1.6 ÷ 3.6 V, V_{ref} = 0.4 V, I_{ref} = 250 nA, and T_j = -40 ÷ 85 °C. Typical values are at V_{avdd} = 2.5 V and T_j = 27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{avdd}	-	1.6	2.5	3.6	V
Operating temperature range	T_j	-	-40	27	85	°C
Output voltage	V_{dvdd}	Trim<5:0>= “011111”, V_{avdd}≥1.85 V	-	1.8	-	V
Trimming range of output voltage	ΔV_{dvdd}	-	±10	-	-	%
Load capacitance	C_{load}	-	-	0.5	-	nF
Max load current	I_{load}	Normal mode, bypass= “0”	30	-	-	mA
		Economy mode, bypass= “0”	3	-	-	
Current consumption	I_{cc}	Normal mode, bypass= “0”	-	20	-	uA
		Economy mode, bypass= “0”	-	5	-	
Input logic-level low	V_{IL}	For digital signals	0	-	0.3*V_{avdd}	V
Input logic-level high	V_{IH}		0.7*V_{avdd}	-	V_{avdd}	

10 TYPICAL CHARACTERISTICS

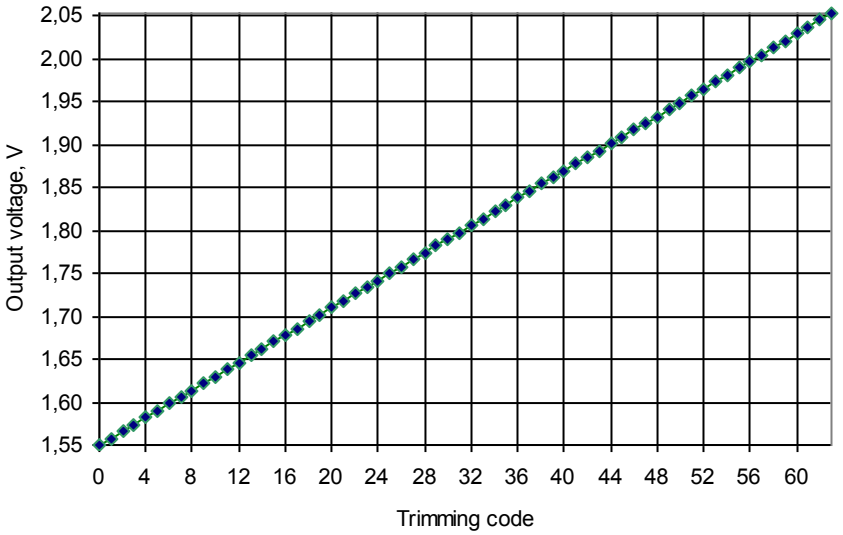

Figure 5: Flash LDO output voltage vs trimming code

11 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

12 REVISION HISTORY

From version 1.0:

- Section 3 “Overview” updated
- Section 4 “Structure” shifted to section 5
- Section 4 “Functional description” added
- Section 5 “Structure”. Figure 3 updated
- Section 6 “Pin description” updated
- Subsection 7.1 “Technology options” updated
- Subsection 7.2 “Physical dimensions”. Figure 4 updated
- Section 8 “Integration guidelines” updated
- Section 9 “Operation characteristics” updated
- Section 10 “Typical characteristics” updated