30mA linear voltage regulator

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- Adjustable output voltage
- High output voltage accuracy
- High power supply rejection ratio
- Small area
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- Battery-powered devices
- Networking and communications

3 OVERVIEW

The voltage regulator is CMOS low dropout linear voltage regulator with 30 mA output current capability. The device have high output voltage accuracy, low supply current and high power supply voltage ripple rejection.

4 STRUCTURE

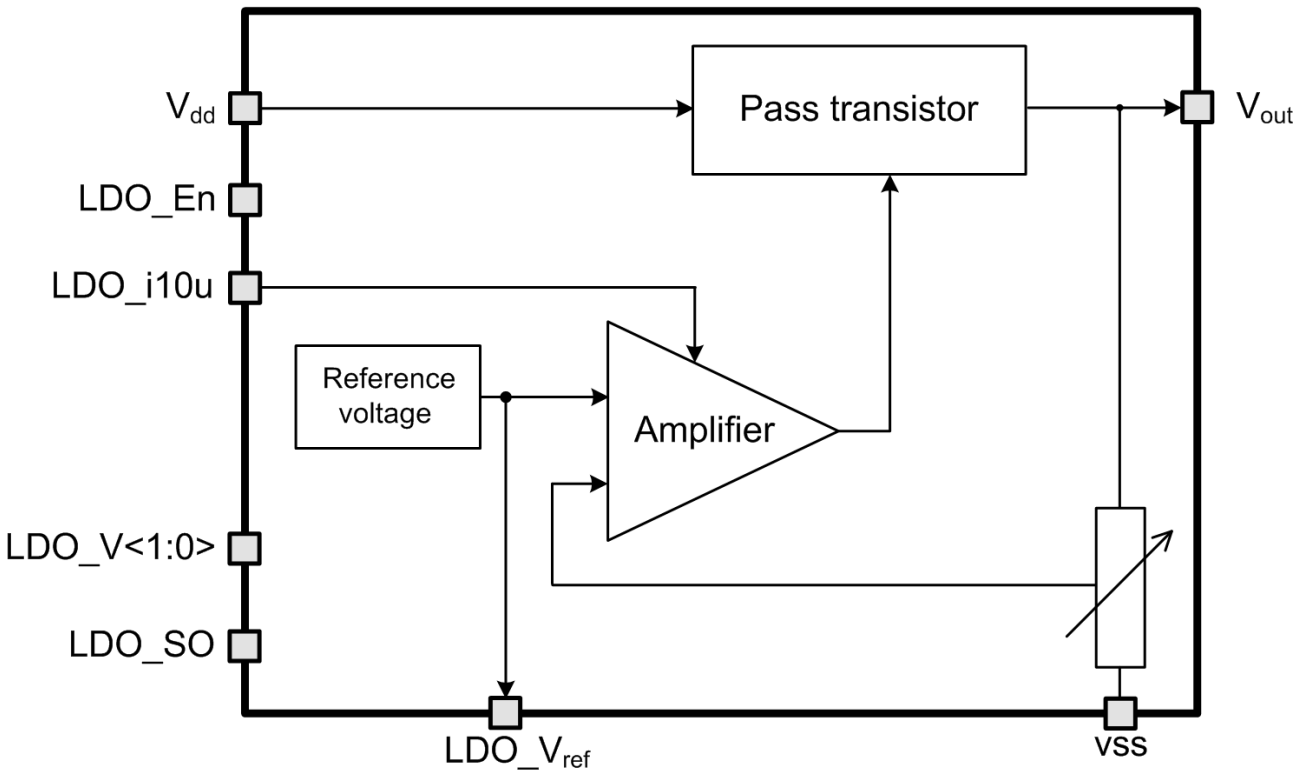

Figure 1: 30mA linear voltage regulator structure

5 PIN DESCRIPTION

Name	Direction	Description
LDO_i10u	I	LDO voltage regulator reference current 10 uA
LDO_En	I	Enable/disable low dropout voltage regulator.
LDO_V<1:0>	I	Output voltage adjustment:
LDO_SO	I	Short out Vout to Vdd line
LDO_V_{ref}	O	LDO reference voltage 1.121 V
V_{dd}	IO	External 2.5V power supply line
V_{out}	IO	LDO voltage regulator output
vss	IO	Ground wire

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	85	µm
Width	235	µm

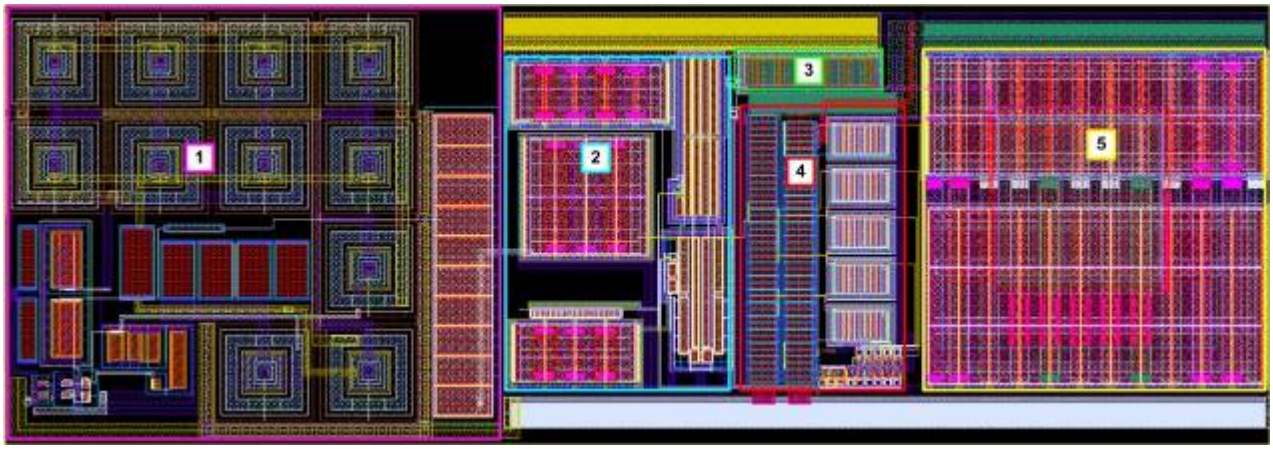

Figure 2: LDOVR layout

1. Bandgap
2. Error Amplifier
3. Regulated p-MOS
4. Adjustable resistive feedback voltage divider
5. Output voltage filtering capacitance

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS CRN65LP
Status silicon proven
Area 0.02 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd} = 2.375÷ 2.625 V and T = -40 ÷ +125°C. Typical values are at V_{dd} = 2.5 V, T = +85 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{dd}	-	2.375	2.5	2.625	V
Temperature range	T	-	-40	+85	+125	°C
Reference voltage	V_{ref}	From bandgap	1.106	1.121	1.134	V
Output voltage	Vdd_pll	LDO preset=1.16 V	1.144	1.164	1.182	V
		LDO preset=1.20 V	1.181	1.200	1.217	
		LDO preset=1.24 V	1.221	1.241	1.257	
		LDO preset=1.28 V	1.283	1.277	1.293	
Line regulation	DV_{line}	Il_{oad} = 1 mA, LDO preset=1.20V	-	1.6	2.0	mV
Load regulation	DV_{load}	LDO preset=1.20V	-	0.7	0.9	mA
Dropout voltage	V_{drop}	I_{load} = 0.1 mA	-	0.004	0.004	V
		I_{load} = 10 mA	-	0.28	0.32	
		I_{load} = 20 mA	-	0.58	0.66	
Short circuit current	I_{sc}	V_{out} = 0	45	60	80	mA
RMS noise	N_f	10Hz - 100kHz, LDO preset=1.20V	-	33	-	uV
Power supply rejection ratio	PSRR	100 Hz	48.8	53.6	-	dB
		10 kHz	48.5	53.1	-	
		1 MHz	21.3	22.1	-	
Linear regulator current consumption	I_{ldo}	-	-	86	88	uA
Bandgap voltage reference current consumption	I_{bg}	-	-	90	120	uA
Standby current	I_{sb}	-	-	2	45	nA
Leackage current	I_{leak}	-	-	35	145	nA
Load current	I_{load}	-	0.1	-	30	mA
Input logic-high level	V_{IH}	-	$0.85V_{dd}$	-	$1.15V_{dd}$	V
Input logic-low level	V_{IL}	-	-0.2	-	0.2	V

8 TYPICAL CHARACTERISTICS

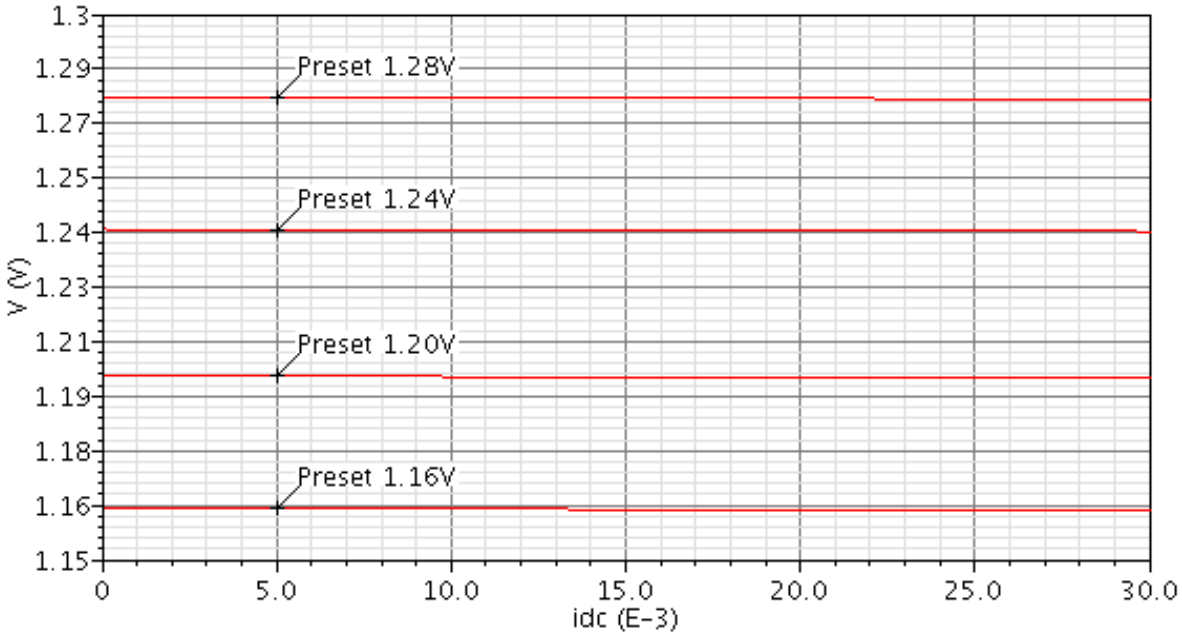

Figure 3: Typical output voltage levels

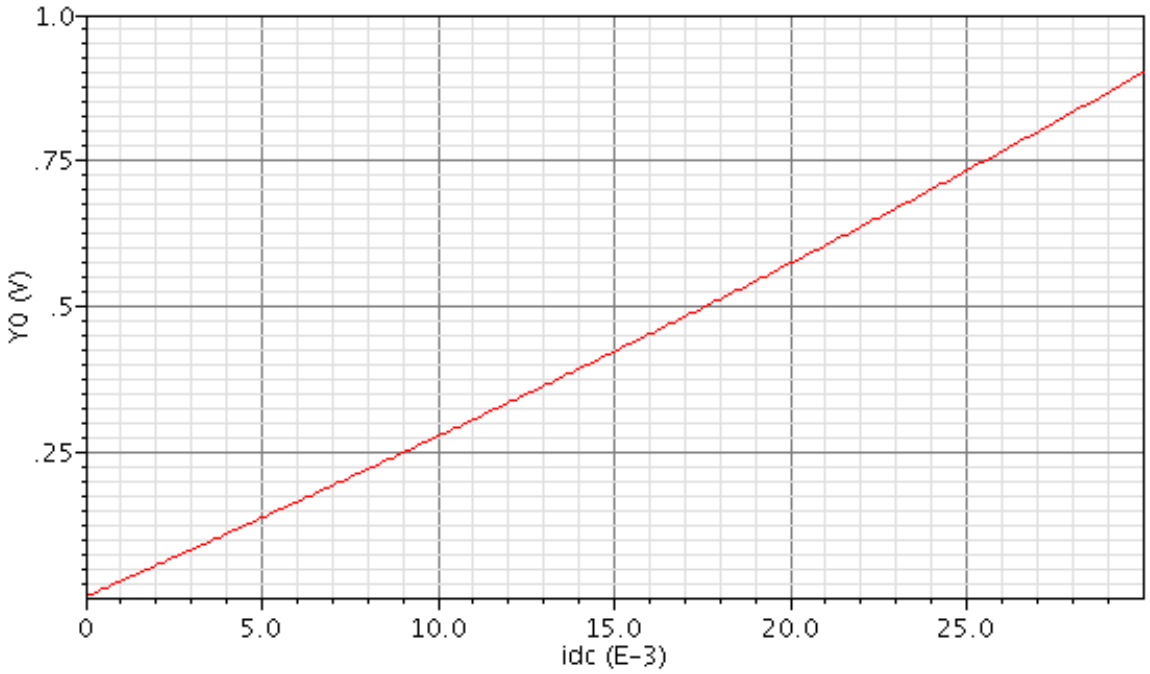

Figure 4: Typical voltage drop vs load current

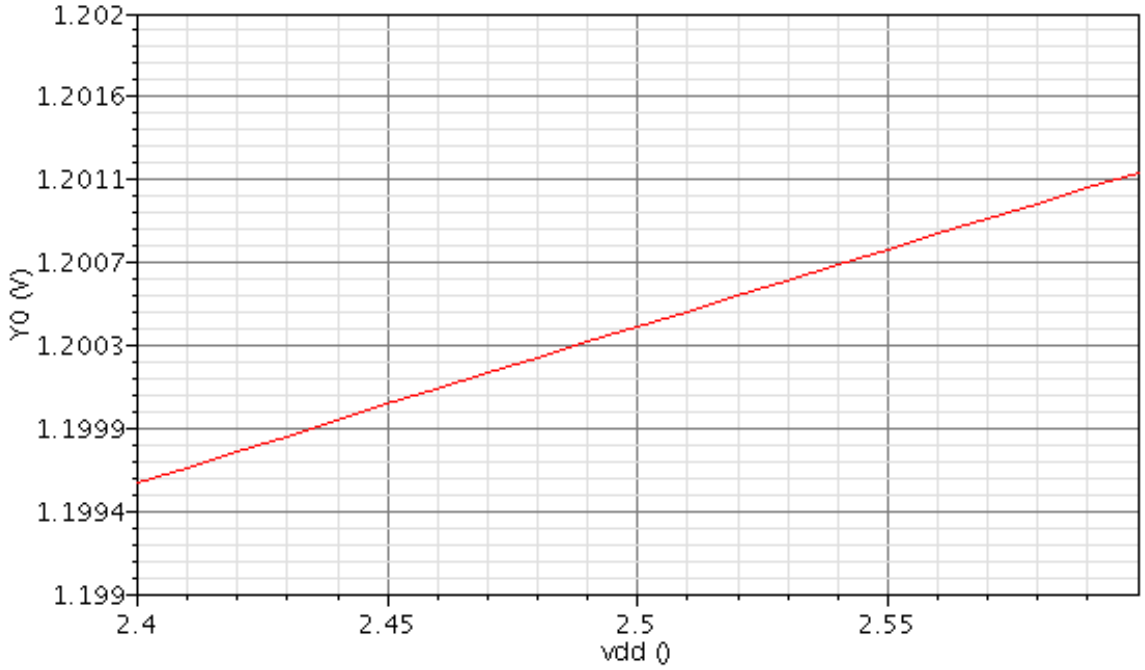

Figure 5: Typical line regulation (output voltage vs input voltage sweep)

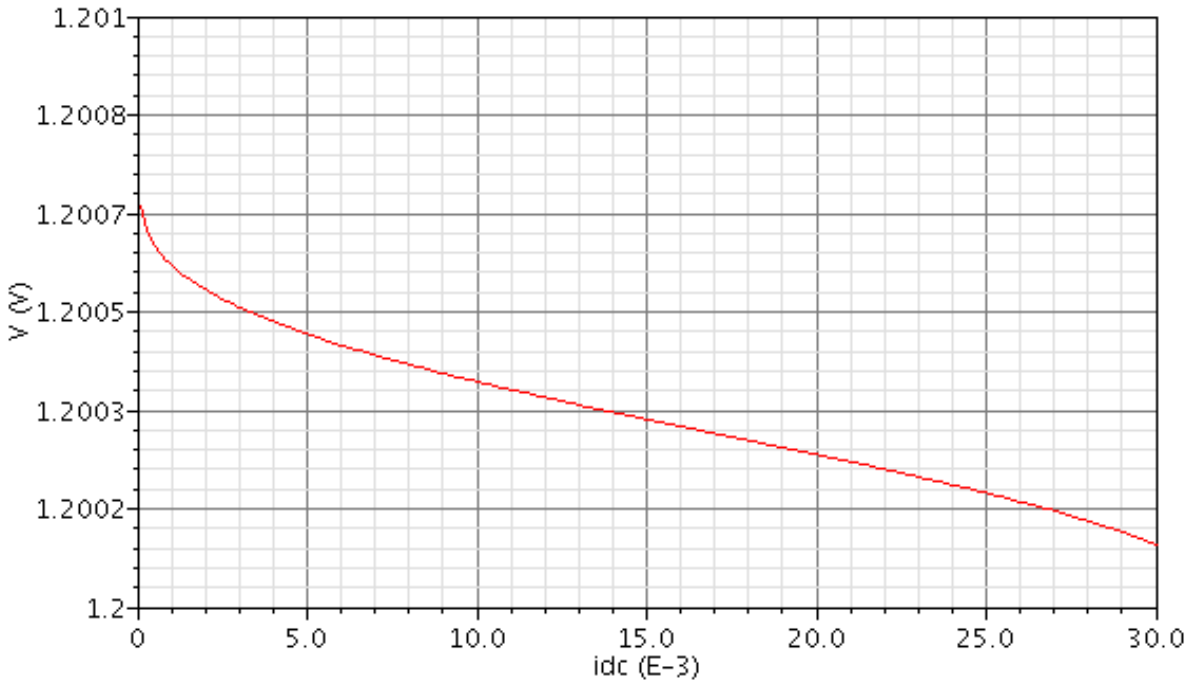

Figure 6: Typical load regulation (output voltage vs load current sweep)

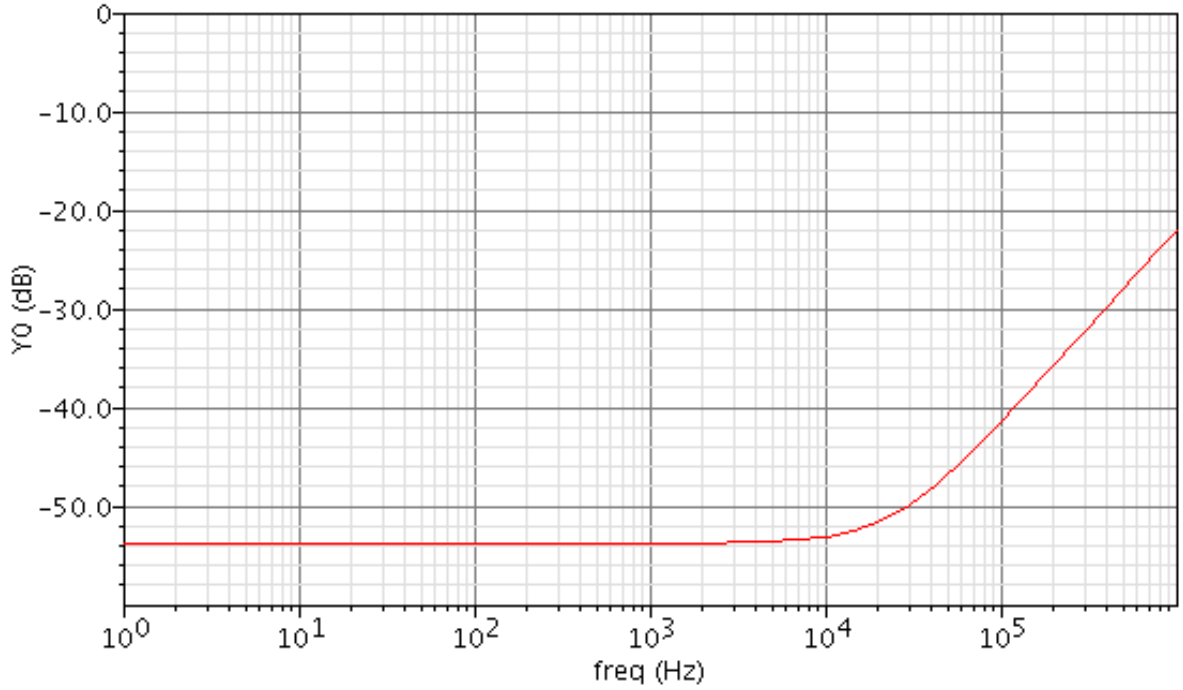

Figure 7: Power supply rejection ration (output vs input voltage ripple)

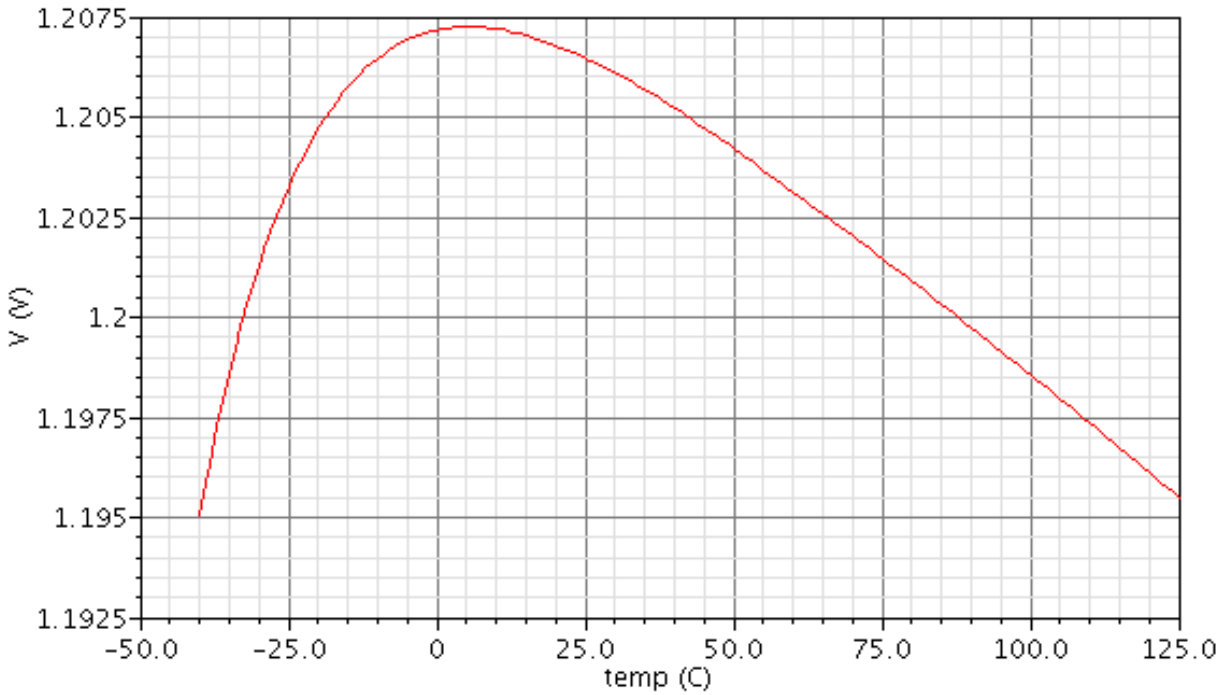

Figure 8: Power supply vs temperature (1,2V LDO output settings)

9 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation