LDO voltage regulator (output voltage value 2.7 V, 3.0 V)

SPECIFICATION

1 FEATURES

- SMIC CMOS 0.18 um
- High precision stabilization voltage
- Several operating modes
- Different output voltage value (2.7 V, 3.0 V)
- Availability of load detection system
- Availability of short circuit detection system
- Ability to control voltage at control transistor
- Low current consumption
- Small area
- Low output level vs. supply voltage in a wide range
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

2 APPLICATION

The output voltage can be used for both analog and digital blocks. The main application:

- Portable electronic devices
- System-on-chip for different purposes
- Measurement and calibration systems
- Navigation systems
- Communication systems

3 OVERVIEW

The regulator stabilizes the external voltage and forms an output level of the specified value. Adjustment is carried out by negative feedback through the operational amplifier. CMOS-transistors keys are used for commutation of different output voltage values. Amplifier output signal is adjusted by the control transistor. There are output bits that allow controlling the regulator by digital interface. Feedback allows for voltage drop on the wire by which stabilized voltage is supplied to the cell.
The block is fabricated on SMIC CMOS 0.18 um technology.

4 STRUCTURE

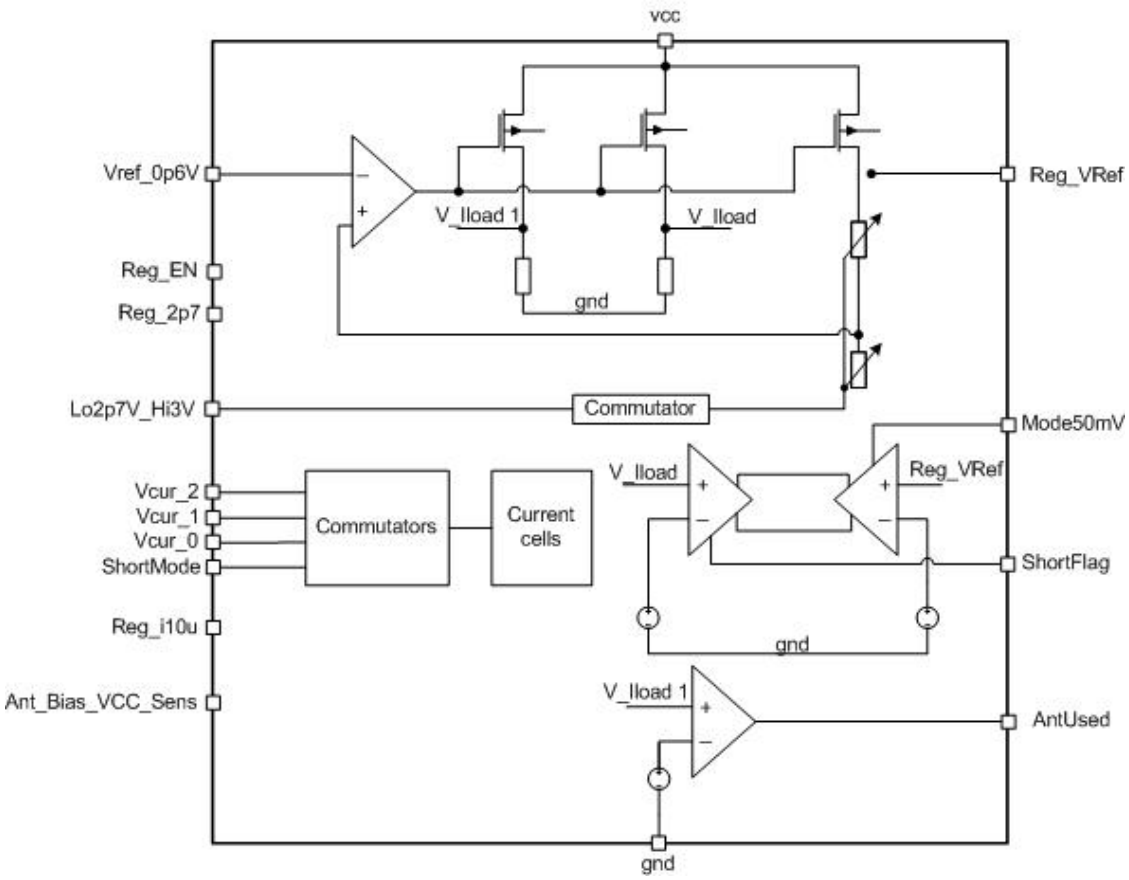

Figure 1: LDO voltage regulator structure

5 PIN DESCRIPTION

Name	Direction	Description
Reg_i10u	I	Reference current 10 uA
Reg_EN	I	Enable/disable
Reg_2p7	I	Output voltage control
Lo2p7V_Hi3V	I	Output voltage digital code control
Vcur_2	I	Digital code controlled the current cells at different current loads
Vcur_1	I	
Vcur_0	I	
ShortMode	I	Control bit that disables block at short circuit
Ant_Bias_VCC_Sens	I	Feedback output
Vref_0p6V	O	Reference voltage
Reg_Vref	O	Output voltage
Mode50mV	O	Output bit that follows the change of voltage at control transistor
ShortFlag	O	Output bit that signals a short circuit
AntUsed	O	Output bit that detects output load
vcc	IO	Supply voltage 3.15 V
gnd	IO	Ground

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	588.06	um
Width	401.94	um

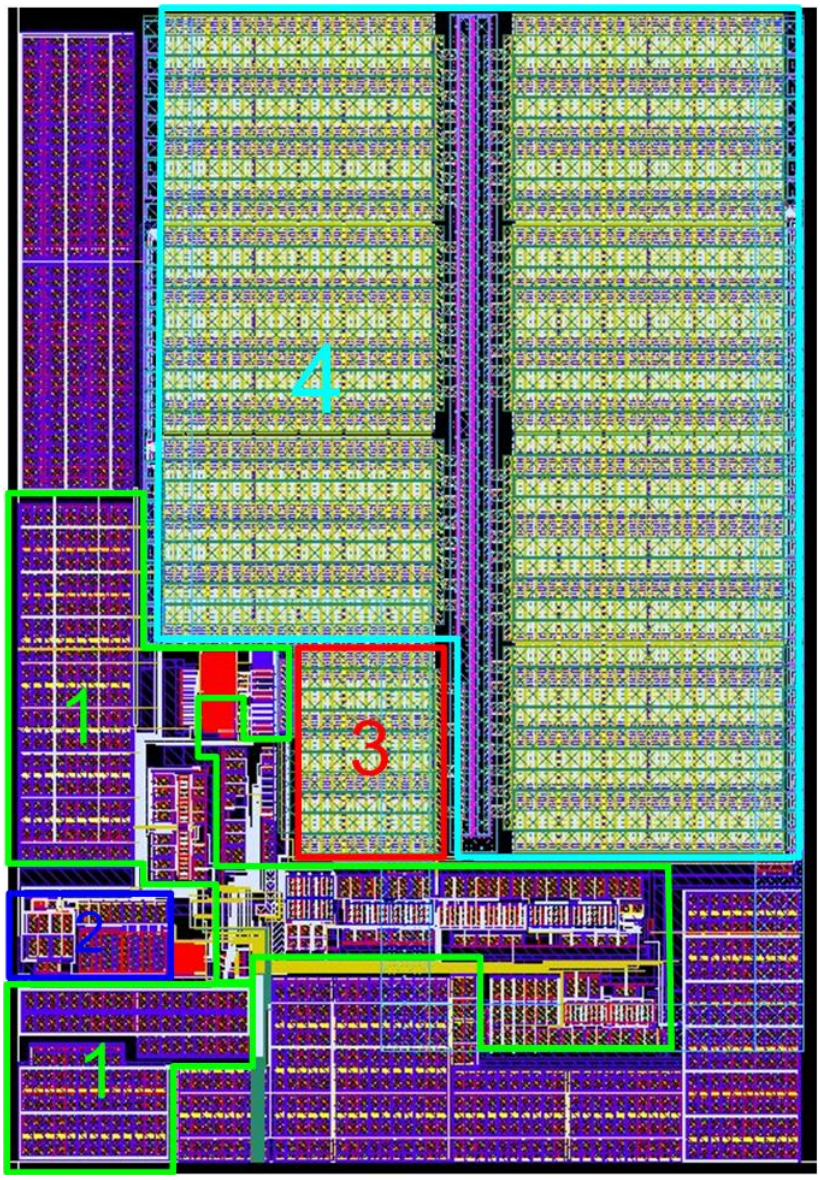

Figure 2: Device layout

1. Current limiting and load detection systems
2. OTA
3. Main control transistor
4. Current cells

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ SMIC CMOS 0.18 um
Status _____ silicon proven
Area _____ 0.24 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.7 ÷ 3.6 V and T_j = -45 ÷ +90 °C. Typical values are at V_{cc} = 3.15 V and T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	2.7	3.15	3.6	V
Operating temperature range	T_j	-	-45	27	90	ºC
Reference voltage	V_R	-	-	0.6	-	V
Voltage regulator output level	V_{ref}	-	2.61	2.7	2.78	V
Reference current	I_R	-	-	10	-	uA
Maximum load current	I_L	-	-	32	-	mA
Reference voltage deviation	ΔV_{ref}	-	-	3.25	-	%
Temperature error	ΔT_j	-	-	0.98	-	%
Current consumption (external supply voltage)	I_{cc}	-	-	197.25	214.1	uA
Current consumption in a standby mode	I_{stb}	-	-	0.34	0.4	nA
Input logic-level high	V_{IH}	For digital inputs	$0.7V_{cc}$	-	3.6	V
Input logic-level low	V_{IL}		-0.25	-	0.3	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

1. From version 1.0:
   - Table “Electrical characteristics” (refer to page 4)