LDO voltage regulator

SPECIFICATION

1 FEATURES

- TSMC018 SiGe BiCMOS 0.18 µm
- Low drop out
- Low current consumption
- Output voltage digital adjustment
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

2 APPLICATION

- Supply voltage sensitive circuits

3 OVERVIEW

The voltage regulator consists of a differential amplifier which compares reference voltage with voltage from a feedback divider. It adjusts the impedance of a pass PMOS transistor for stabilization of output voltage at a set level. The output voltage adjustment is defined by the digital code OV<1:0>. It is able to change a feedback divider transfer ratio in range of 0.6 / 0.7 / 0.8 / 0.9.
The block is fabricated on TSMC018 SiGe BiCMOS 0.18 µm technology.

4 STRUCTURE

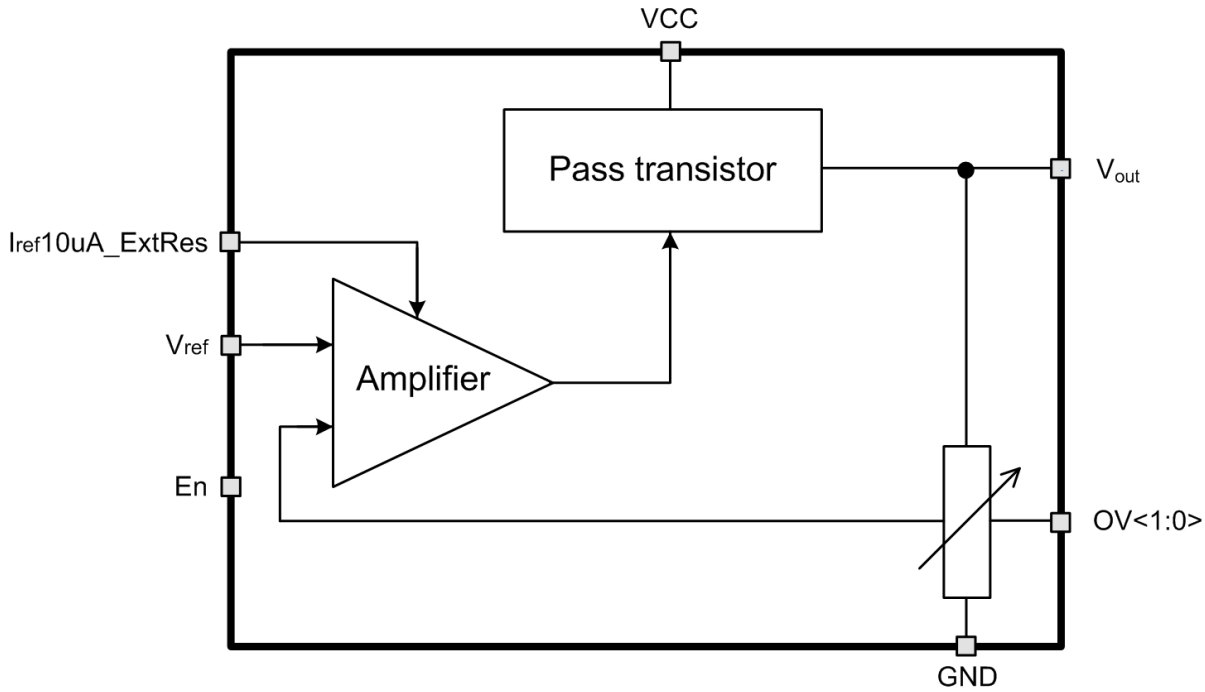

Figure 1: LDO voltage regulator structure

5 PIN DESCRIPTION

Name	Direction	Description
I_{ref}10uA_ExtRes	I	Reference current 10 µA
V_{ref}	I	Reference voltage
OV<1:0>	I	Digital code of output voltage adjustment
En	I	Enable/disable
V_{out}	O	Output voltage
VCC	IO	Supply voltage
GND	IO	Ground

6 LAYOUT DESCRIPTION

Programmable LDO voltage regulator dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	80	µm
Width	120	µm

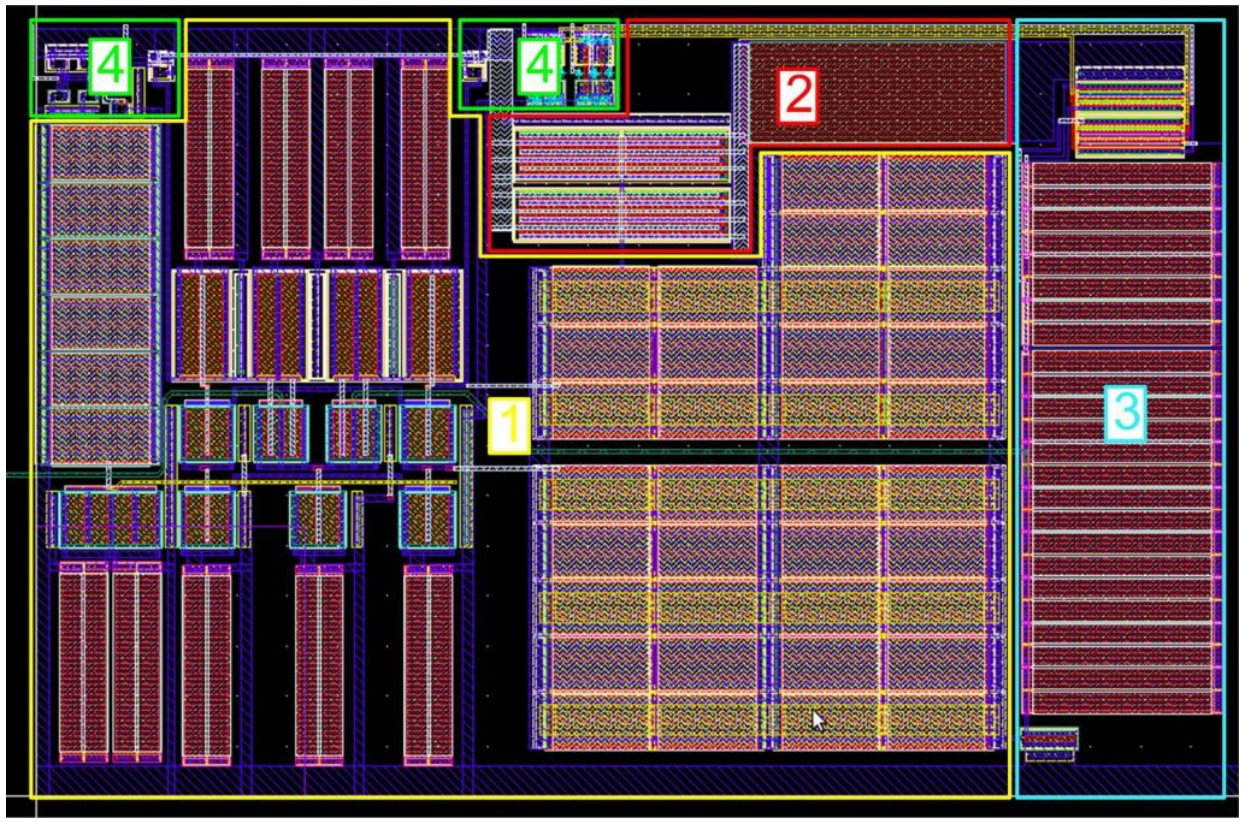

Figure 2: Programmable LDO voltage regulator layout

1. Differential amplifier
2. Pass transistor
3. Feedback divider
4. Control logic

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC018 SiGe BiCMOS
Status _____ Silicon proven
Area _____ 0.01 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for Vcc= 2.4 ÷ 3.6 V и T = -40 ÷ +85°C. Typical values are at V_{CC} = 3.0 V, T = +27°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	2.4	3.0	3.6	V
Operating temperature range	T	-	-40	+27	+85	°C
Reference voltage	V_{ref}	-	0.9	1.16	-	V
Maximum load current	I_{out}	-	-	-	2	mA
Output voltage	V_{out}	OV<1:0>= “00”	-	1.6× V_{ref}	-	V
		OV<1:0>= “01”		1.7× V_{ref}		
		OV<1:0>= “10”		1.8×V_{ref}		
		OV<1:0>= “11”		1.9× V_{ref}		
Supply current	I_{cc}	-	-	30	-	uA
Stand-by current	I_{st}	-	-	1	-	nA
Input logic-level high	V_{OH}	For digital inputs	0.9V_{cc}	-	1.1V_{cc}	V
Input logic-level low	V_{OL}		-0.2	-	0.2	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation