

## LDO voltage regulator (output voltage 2.7 V)

### SPECIFICATION

#### 1 FEATURES

- AMS035 BiCMOS 0.35  $\mu\text{m}$
- Low drop out voltage
- Low own current consumption
- External voltage to output short out mode
- Standby mode
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

#### 2 APPLICATION

- Combination of low drop out voltage with low own current consumption and simplicity allow to use scheme to regulate voltage in portable devices with battery power source.

#### 3 OVERVIEW

The voltage regulator consists of differential amplifier which compares reference voltage with voltage from feedback divider. It adjusts the impedance of the pass PMOS transistor for stabilization of output voltage at the set level.

The block is fabricated on AMS035 BiCMOS 0.35  $\mu\text{m}$  technology.

#### 4 STRUCTURE

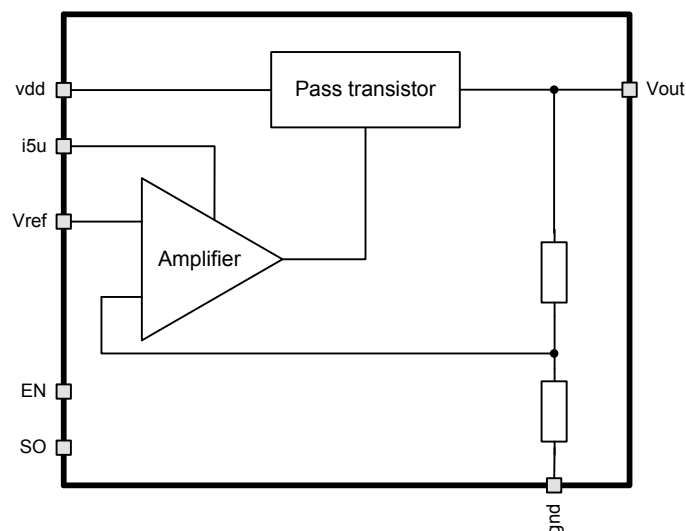


Figure 1: LDO voltage regulator structure

## 5 PIN DESCRIPTION

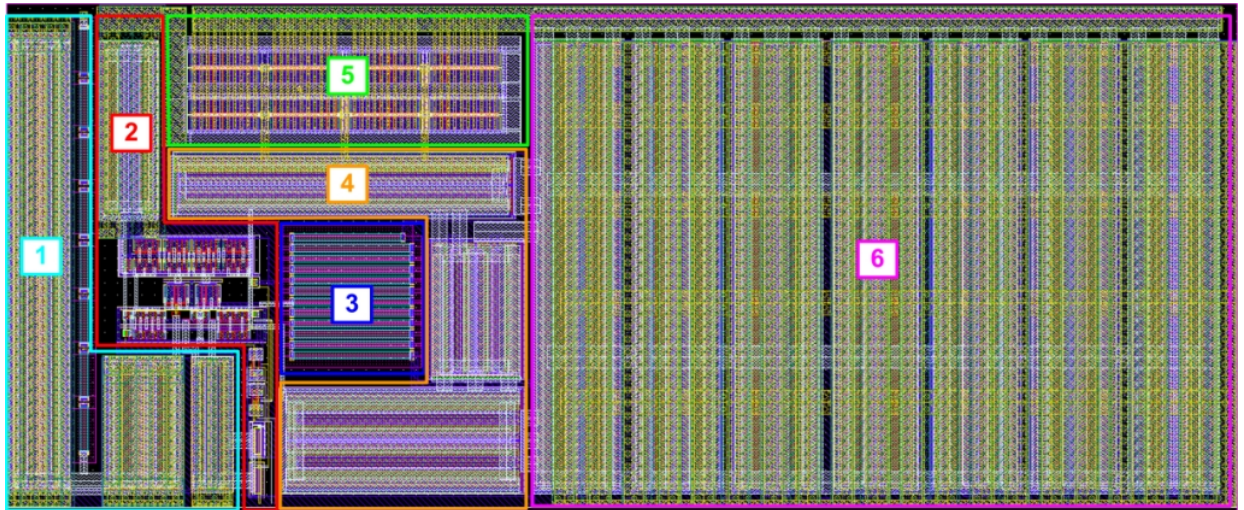
Name	Direction	Description
Vout	I	Output voltage
Vref	I	Reference voltage
i5u	I	Reference current 5 $\mu$ A
EN	I	Voltage regulator enable/disable
SO	I	Supply external voltage to output mode
vdd	IO	Supply voltage
gnd	IO	Ground

## 6 LAYOUT DESCRIPTION

LDO voltage regulator dimensions are given in the table 1.

**Table 1:** Block dimensions

Dimension	Value	Unit
Height	120	$\mu\text{m}$
Width	147	$\mu\text{m}$



**Figure 2:** LDO voltage regulator layout

1. Input reference voltage LPF
2. Differential amplifier
3. Feedback divider
4. Stabilizing capacity
5. Regulate transistor
6. Output voltage filtration capacity

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ AMS035 BiCMOS 0.35  $\mu\text{m}$   
 Status \_\_\_\_\_ silicon proven  
 Area \_\_\_\_\_ 0.1mm<sup>2</sup>

### 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{cc} = 2.85 \div 3.15 \text{ V}$ ,  $T = -40 \div +85^\circ\text{C}$ . Typical values are at  $V_{cc} = 3.0 \text{ V}$ ,  $T = +27^\circ \text{C}$ , unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	$V_{in}$		2.85	3.0	3.15	V
Reference voltage	$V_{ref}$	-	-	1.13	-	V
Reference current	$I_{ref}$	-	-	5	-	$\mu\text{A}$
Output voltage	$V_{out}$	-	-	2.7	-	V
Operating temperature range	T		-40	27	85	$^\circ\text{C}$
Maximum load current	$I_{load\ max}$	-	-	20	-	mA
Own current consumption	$I_c$	-	25	30	35	$\mu\text{A}$
The output voltage dependence of the input	$D_{vout}$	$I_{load} = 1 \text{ mA}$	-0.25	-	0.25	%
Stand-by current	$I_{sb}$	-	-	<1	-	nA
Input logic-level high	$V_{IH}$	For digital inputs	$0.9V_{cc}$	-	3.15	V
Input logic-level low	$V_{IL}$	$V_{adj} < 1:0 >$ and En	-0.2	0	0.2	V

## 8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

## REVISION HISTORY

1. From version 1.0:
  - Section “Technical characteristics” (refer to [page 4](#))