

## Low - pass filter with frequency adjustment system

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### SPECIFICATION

#### 1 FEATURES

- SMIC CMOS 0.18 $\mu$ m
- Wide cut-off frequency adjustment range (1MHz...200MHz)
- Low group delay time ripple vs. frequency (3.5ns)
- Low pass filter cut-off frequency adjustment system (LPF CFAS)
- There are 4 operation modes
- No external components required
- Portable to other technologies (upon request)

#### 2 APPLICATION

- Intermediate frequency signal processing
- Navigation systems including multisystems

#### 3 OVERVIEW

The cell is based on 3<sup>rd</sup> order Butterworth low-pass filter (LPF) with cut-of frequency adjustment in a wide range. There are 2 modes for cut-off frequency programming: manual and automatically. The generator is used to control filter cut-off frequency in an automatic mode. Oscillator oscillation frequency correlates with cut-off frequency which can be fixed by digital code LPF\_ctrl<6:0>.

There are 4 operation modes with different rated signal level under the same value of distortion. Greater level of signal corresponds to a higher current consumption.

It is possible to use several LPF with one generator for multichannel systems.

The block is fabricated on SMIC CMOS 0.18 $\mu$ m technology.

## 4 STRUCTURE

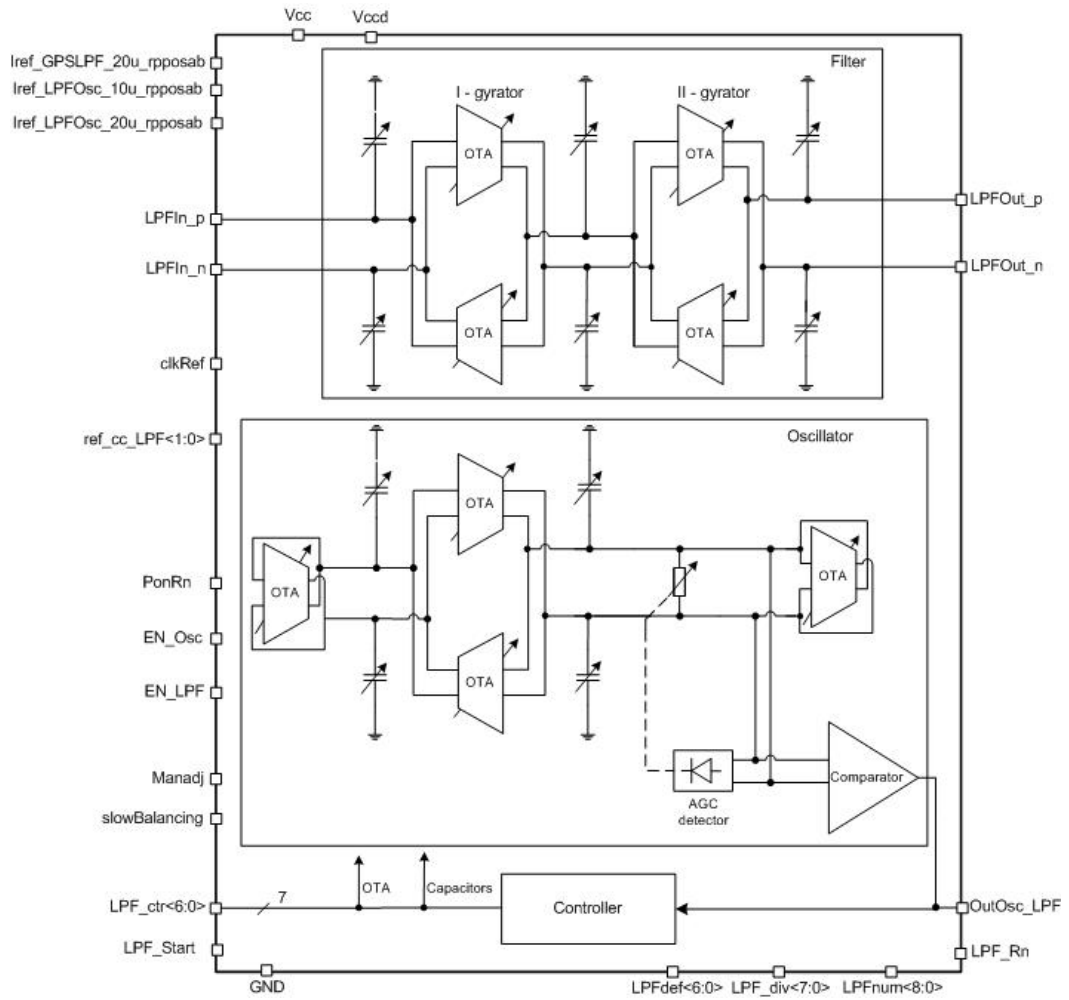


Figure 1: Low-pass filter with frequency adjustment system structure.

## 5 PIN DESCRIPTION

Name	Direction	Description
LPFIn_p	I	Analog differential input
LPFIn_n	I	
LPF_ctr<6:0>	O	Digital code controlling a central frequency
LPFdef<6:0>	I	Digital input of LPF cut-off frequency adjustment system
LPF_div<7:0>	I	Digital code forming coefficient for frequency adjustment system
LPF_num<8:0>	I	Pulse number for internal LPF adjustment
clkRef	I	Reference frequency (3.105 MHz)
ref_cc_LPF<1:0>	I	Reference voltage control
slowBalancing	I	Oscillator setting time control
Iref_GPSLPF_20uA_rposab	I	Reference current (20 $\mu$ A)
Iref_LPFOsc_10uA_rposab	I	Reference current (10 $\mu$ A)
Iref_LPFOsc_20uA_rposab	I	Oscillator reference current (20 $\mu$ A)
Manadj	I	Manual mode enable for cut-off frequency adjustment enable
PonRn	I	Reset of defaults
EN_Osc	I	Oscillator enable/disable
EN_LPF	I	LPF enable/disable
LPF_Start	I	Filter automatic frequency adjustment system enable
LPFOut_p	O	Analog differential output
LPFOut_n	O	
OutOsc_LPF	O	Oscillator digital output
LPF_Rn	O	Automatic adjustment system status
Vccd	IO	Digital supply voltage
Vcc	IO	Supply voltage
GND	IO	Ground

## 6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

**Table 1:** Block dimensions.

Dimension	Value	Unit
Height	441.54	$\mu\text{m}$
Width	384.45	$\mu\text{m}$

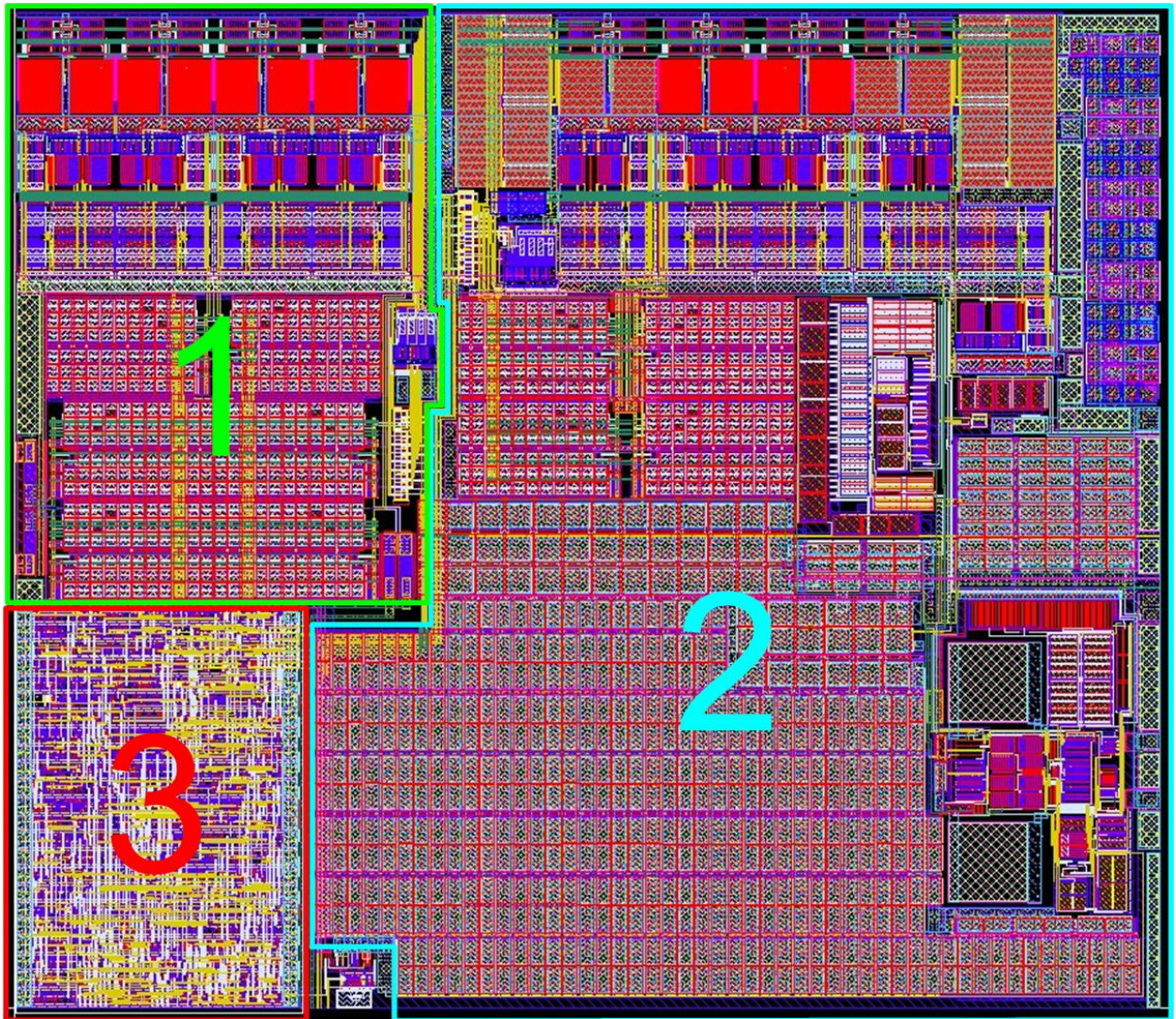


Figure 2: Device layout view.

1. LPF
2. Oscillator
3. Controller

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ SMIC CMOS 0.18 $\mu$ m  
 Status \_\_\_\_\_ silicon proven  
 Area \_\_\_\_\_ 0.17mm<sup>2</sup>

### 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{cc} = 1.7 \div 1.9$  V ,  $V_{dd} = 2.7 \div 3.6$  V and  $T = -45 \div +90$  °C. Typical values are at  $V_{cc} = 1.8$  V,  $V_{dd} = 3.15$  V and  $T = +27$ ° C , unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	$V_{cc}$	-	1.7	1.8	1.9	V
Digital supply voltage	$V_{dd}$	-	2.7	3.15	3.6	V
Operating temperature range	T	-	-45	27	90	°C
Filter order	k	-	-	3	-	-
Insertion loss	G	-	-	-0.3	-	dB
Input signal bandwidth	F	-	-	18.07	-	MHz
Attenuation factor	$\alpha$	At 25MHz	-	8.05	-	dB
		At 50MHz	-	24.08	-	
		At 100MHz	-	41.73	-	
Group delay time ripple	$t_{del}$	-	-	2.48	-	ns
Noise figure	NF	-	-	16.18	-	dB
Input 1dB compression point	$P_{1dB}$	-	-	-21.26	-21.54	dBm
Input impedance	$R_{in}$	At differential input	-	2	-	k $\Omega$
Output impedance	$R_{out}$	At differential output	-	2	-	k $\Omega$
Oscillator start time	$t_{start}$	-	-	-	1.5	ms
Peak-to-peak oscillator analog signal	A	-	-	120	-	mV
Oscillation frequency range	F	-	7	-	150	MHz
LPF offset error	$\delta$	-	-	-	5	%
Current consumption	$I_{cc}$	-	-	1.3	1.5	mA
Current consumption in a standby mode	$I_{stb}$	-	-	-	1.1	$\mu$ A
Input logic-high level	$V_{IH}$	For digital inputs	$0.7 V_{cc}$	-	3.6	V
Input logic-low level	$V_{IL}$		-0.25	-	0.3	V

## 8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation