CML Receiver

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- 1.2 V digital power supply
- 2.5 V CMOS input logic signals
- 1.2 V CMOS output logic signals
- 3.125 Gbps (DDR MODE) switching rates
- Temperature range: -40 °C to + 125 °C
- Optimized for pad-limited layout design
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- Point-to-point data transmission
- Multidrop buses
- Clock distribution
- Backplane receiver
- Backplane data transmission
- Cable data transmission

3 OVERVIEW

The block is a CML receiver. Core logic interface includes complementary output signal pins (OUTp, OUTn) for data transmission and enable pin (EN_RX). PAD_INp and PAD_INn are differential input pins that should be connected to bonding pads. Buffer includes two 50-Ohm on-chip termination resistors, connected to supply voltage node. So the interface supports both AC and DC-coupled connections. IREF_RX is a reference current input.
The CML receiver is designed using TSMC CMOS 65 nm technology.

4 STRUCTURE

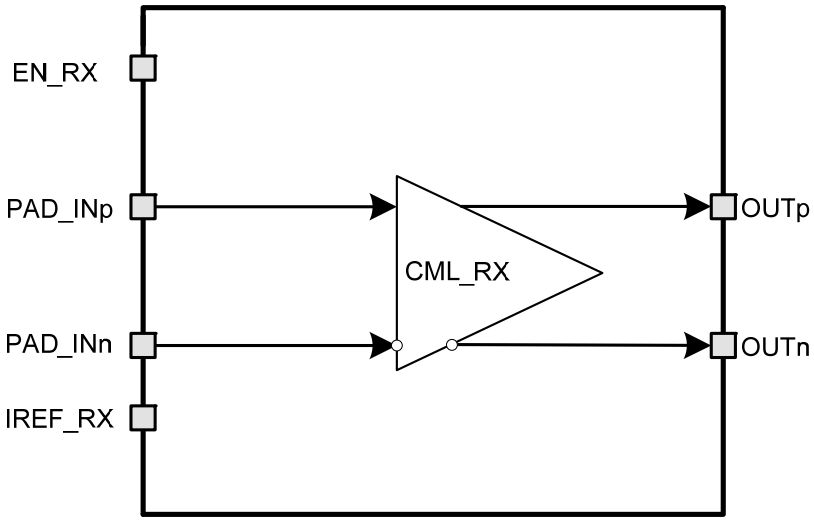

Figure 1: 3.125 Gbps CML receiver structure.

5 PIN DESCRIPTION

Name	Direction	Description
IREF_RX	I	Reference current
PAD_INp	I	Input differential CML signal
PAD_INn		
EN_RX	I	CML receiver enable
OUTp	O	Output complementary CMOS signals
OUTn		

Table 1: CML receiver truth table.

Mode	Input			Output	
	EN_RX	PAD_INp	PAD_INn	OUTp	OUTn
Receive	1	1	0	1	0
		0	1	0	1
Power down	0	X	X	1	0

6 LAYOUT DESCRIPTION

CML receiver dimensions are given in the table 2.

Table 2: Block dimensions.

Dimension	Value	Unit
Height	39.5	um
Width	120	um

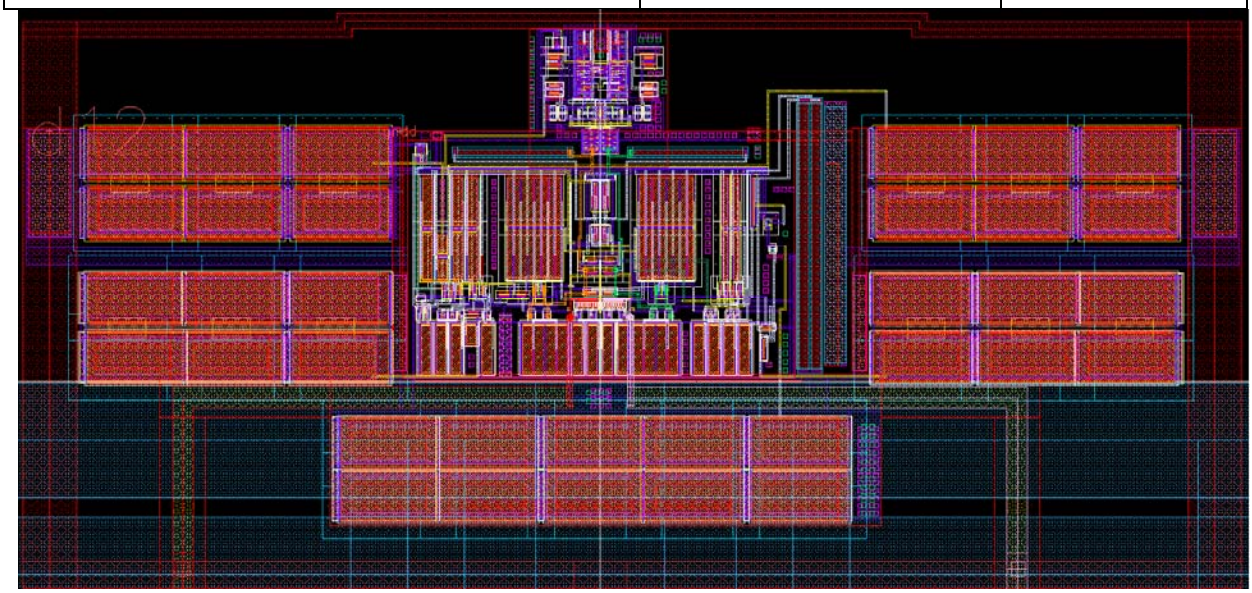

Figure 2: 3.125 Gbps CML receiver layout view.

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC 65 nm CMOS
Status silicon proven
Area 0.01 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd}= 1.14 ÷ 1.26 V and T = -40 ÷ +125 °C. Typical values are at V_{dd}= 1.2 V, T=+85 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{dd}	-	1.14	1.2	1.26	V
Operating temperature range	T	-	-40	+85	+125	°C
Input voltage range (common-mode)	V_{in}	-	1.14	1.2	1.26	V
Input differential threshold	V_{th}	-	100	400	-	mV
DC power current from V_{dd25}	I_{VDD25}	IREF_RX = 40 uA	0.98	0.99	1.03	mA
Total DC power	P_{total}		1.11	1.19	1.30	mW
Stand-by current	I_{st}	-	136.0	381.7	432.2	nA
Output voltage range	V_{out}	-	0	-	1.25	V
Differential time propagation delay, high to low	t_{PHLDT}	-	638.7	648.3	652.3	ps
Differential time propagation delay, low to high	t_{PLHDT}	-	634.8	646.1	657.4	ns
AC power current from V_{dd25}	I_{VDD25}	IREF_RX = 40 uA	1.20	1.37	1.40	mA
Total AC power	W	IREF_RX = 40 uA	1.37	1.64	1.76	mW
Clock jitter, rms	t_{RJ}	Ampl_in = 0.12 V	1.10	1.57	2.65	ps
Clock jitter, max (p-p)	t_{DJM}		1.55	2.21	3.74	ps
Data jitter, deterministic	t_{DJ}	Ampl_in = 0.12 V	42.61	42.77	62.98	ps

8 TYPICAL CHARACTERISTICS

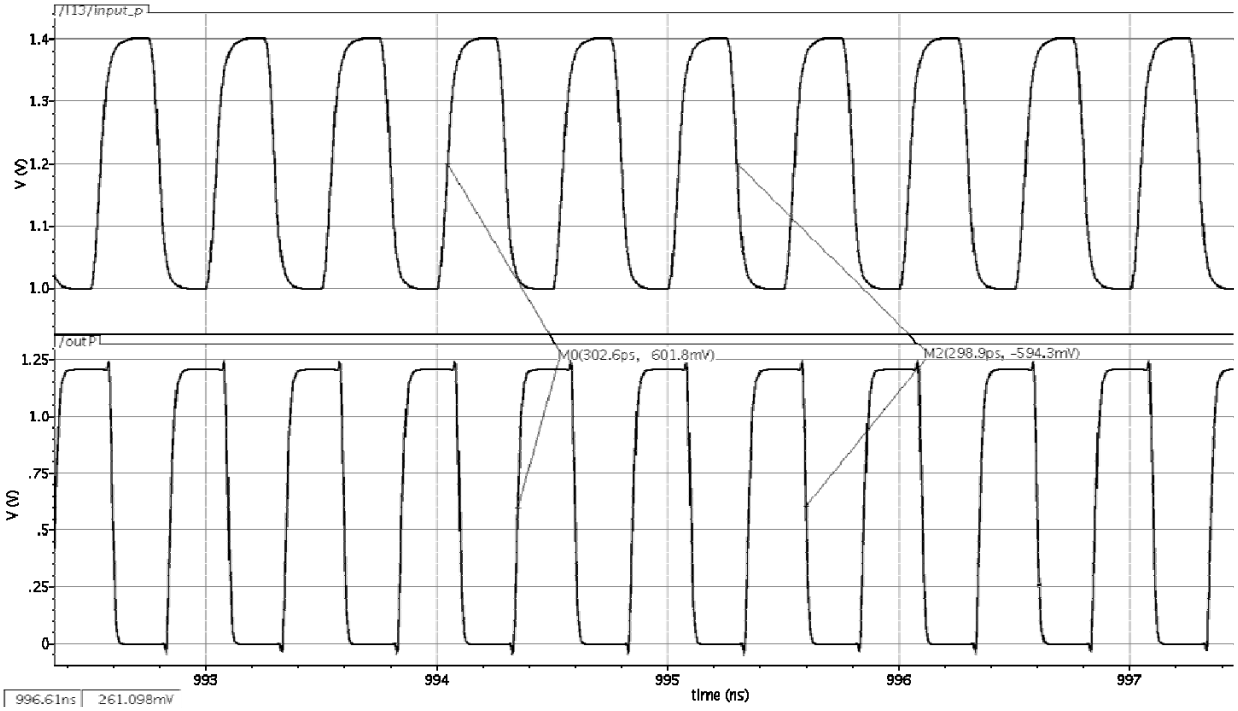

Figure 3: The time diagram of the receiver by clock input signal, Fin = 2 GHz.

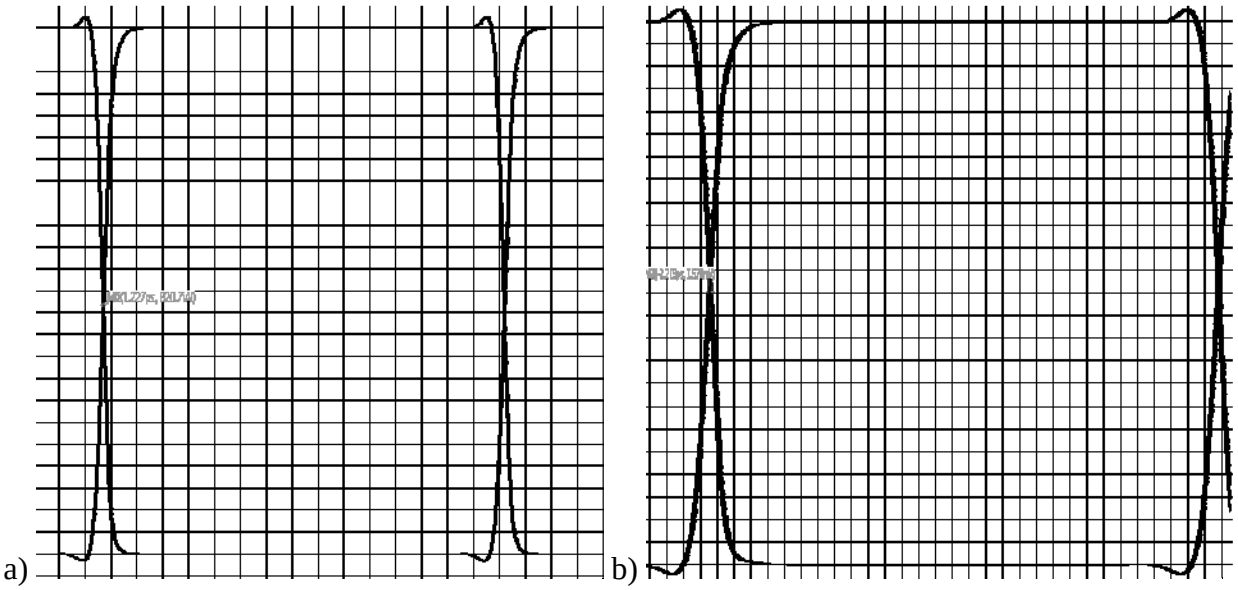

Figure 4: The “eye” diagram of the receiver by clock input signal, Fin = 1.625 GHz:
a) schematic; b) extraction.

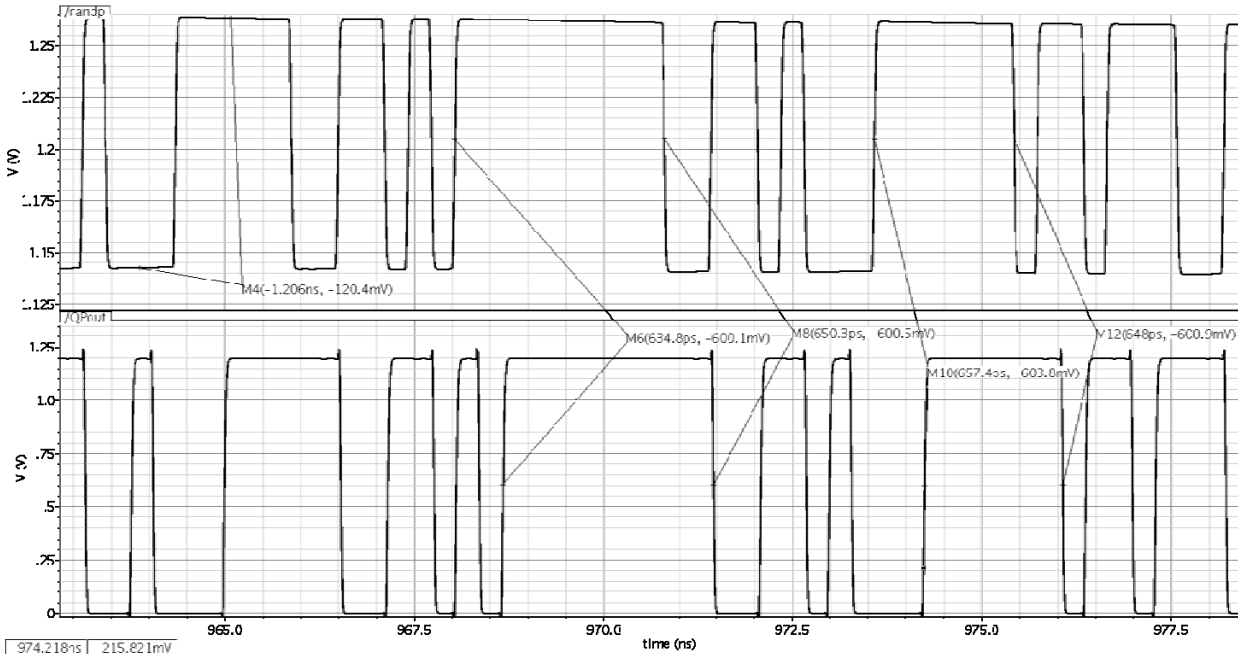

Figure 5: The time diagram of the receiver by random input signal, Fin(max) = 1.625 GHz. Modeling of extraction.

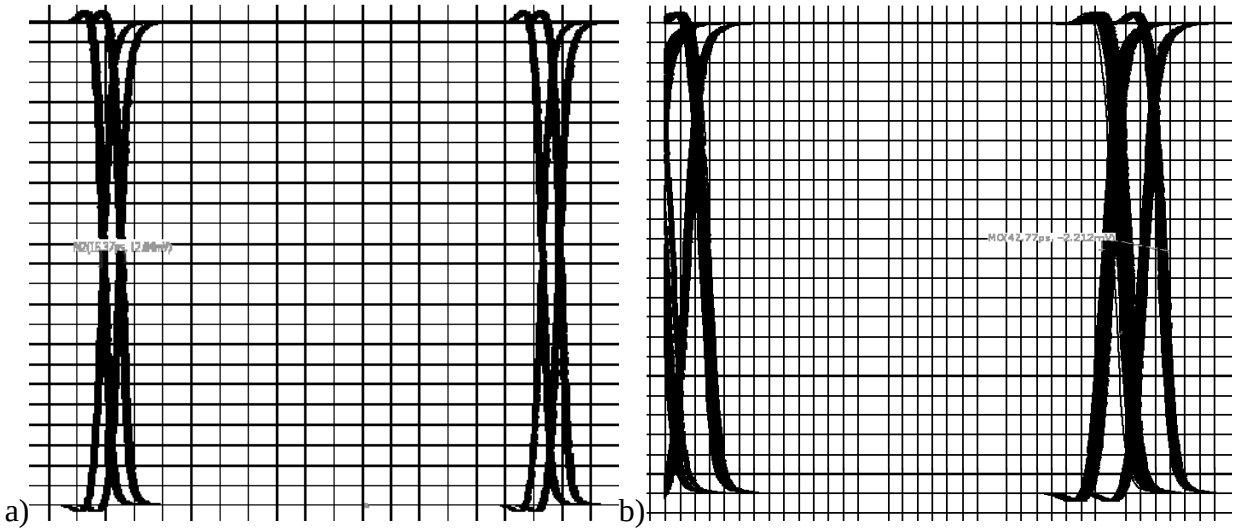

Figure 6: The “eye” diagram of the receiver by random input signal, Fin(max) = 1.625 GHz.
a) schematic; b) extraction.

9 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation