LVDS Transmitter

SPECIFICATION

1 FEATURES

- TSMC CMOS 0.065 um
- 2.5 V analog power supply
- 1.2 V digital power supply
- 1.2 V CMOS input logic signals
- 4-step (2-bit) adjustable transmitter output current range (from 1.75 mA to 7.0 mA)
- 1 Gbps (DDR MODE) switching rates
- Conforms to TIA/EIA-644 LVDS standards without hysteresis
- Temperature range: -40 °C to + 125 °C
- Optimized for pad-limited layout design
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- Point-to-point data transmission
- Multidrop buses
- Clock distribution
- Backplane data transmission
- Cable data transmission

3 OVERVIEW

The interface to the core logic includes signal pins (INp and INn) to transmit data, and control pin EN_TX to configure the state of the transmitter. There are other two internal pins (VREF_TX and IREF_TX) to get voltage reference and current reference. PAD_OUTp and PAD_OUTn are complementary outputs to connect to the bonding pads.

4 STRUCTURE

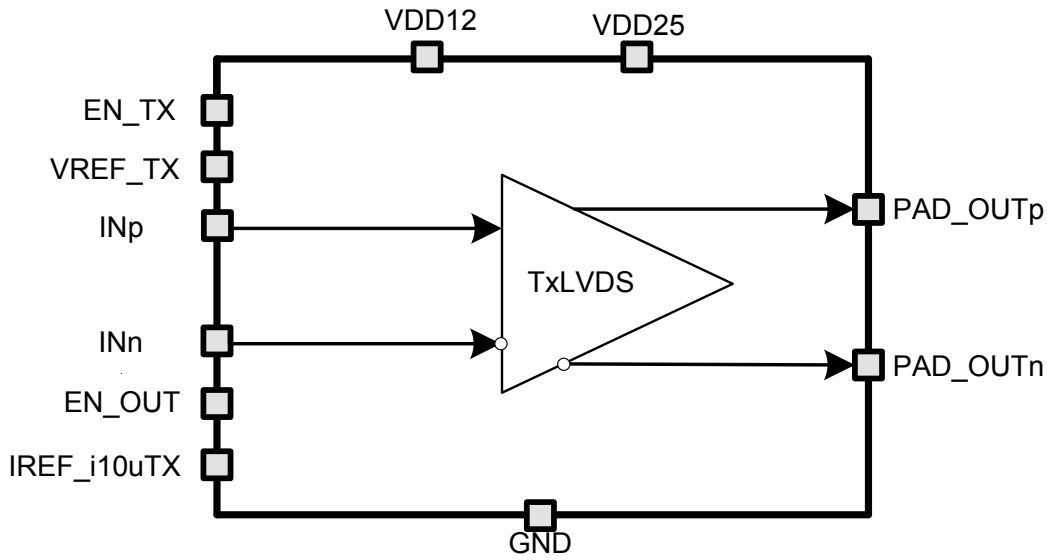

Figure 1: LVDS Transmitter structure.

5 PIN DESCRIPTION

Name	Direction	Description
IREF_i10uTX	IO	Reference current 10uA
VREF_TX	I	Reference voltage
EN_OUT	I	Transmitter enable/disable
EN_TX	I	LVDS transmitter enable
INp	I	Input differential LVDS signal
INn	I	
PAD_OUTp	O	Output differential LVDS signal of transmitter
PAD_OUTn		
VDD12	IO	Supply voltage 1.2 V
VDD25	IO	Supply voltage 2.5 V
GND	IO	Ground

Table 1: LVDS transmitter truth table.

Mode	Input		Output	
	EN_TX	INp	PAD_OUTp	PAD_OUTn
Transmit	1	0	0	1
		1	1	0
Power down	0	X	Z	Z

6 LAYOUT DESCRIPTION

LVDS transmitter dimensions are given in the table 2.

Table 2: Block dimension.

Dimension	Value	Unit
Height	106	um
Width	146	um

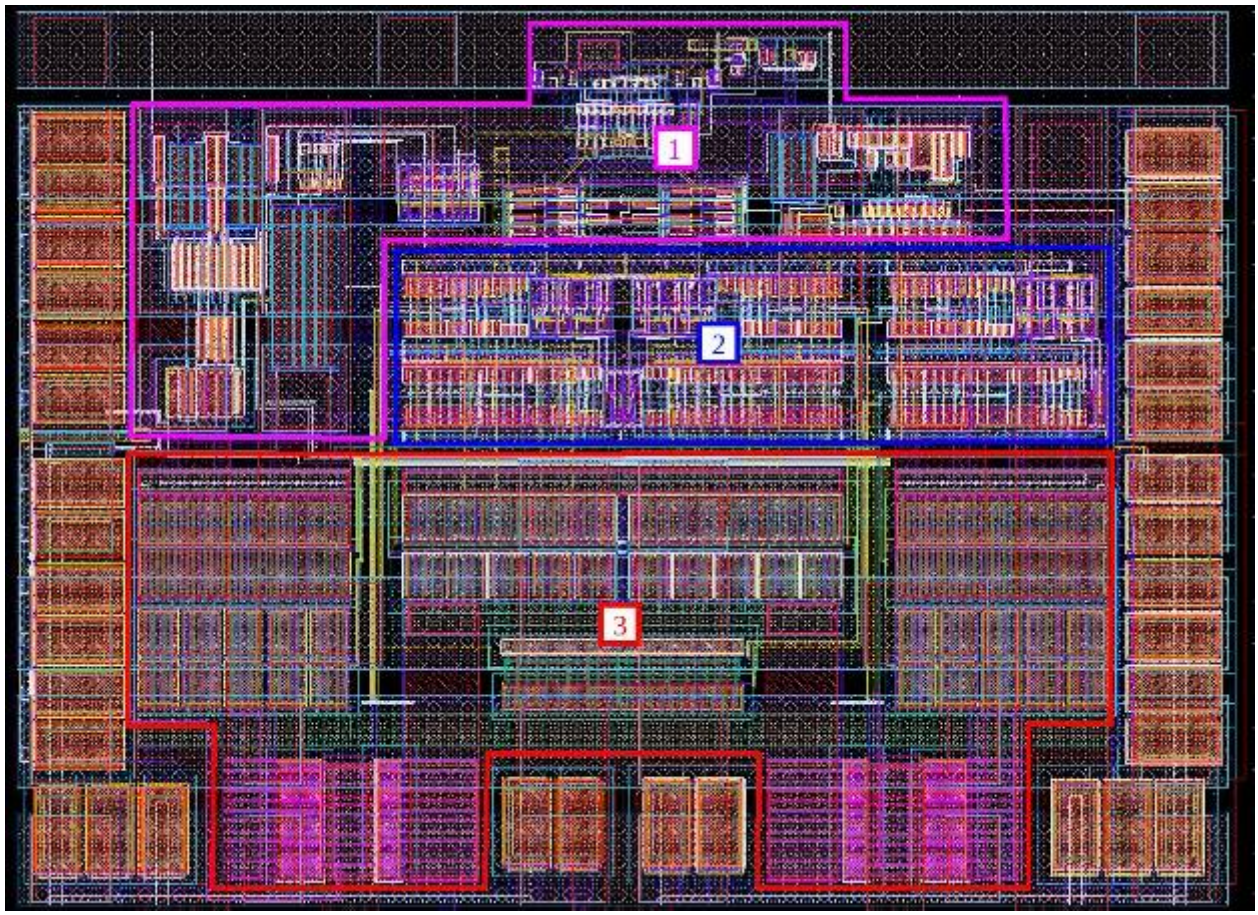

Figure 2: LVDS transmitter layout view.

1. Digital control
2. Digital buffer
3. Output stage

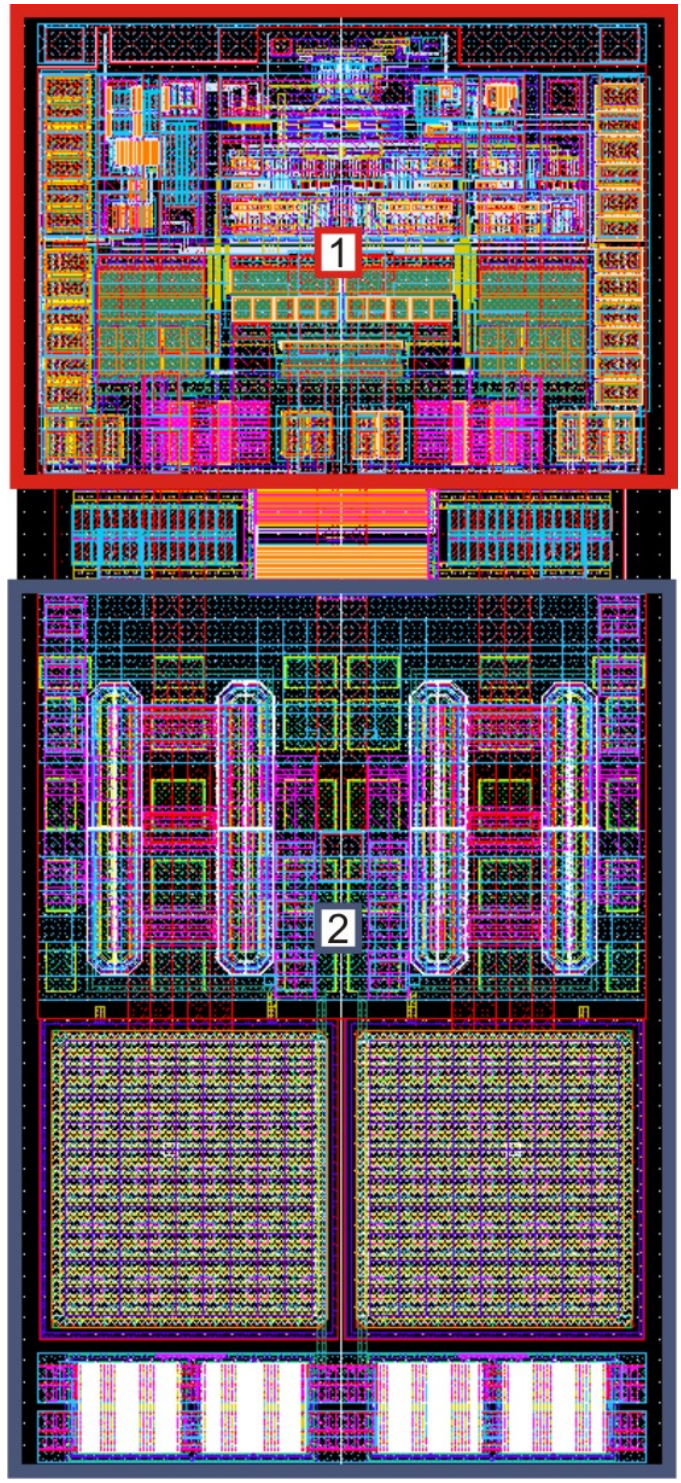

Figure 3: PAD oriented layout view.

1. LVDS transmitter
2. PAD with ESD protection

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC 0.065um CMOS
Status _____ silicon proven
Area _____ 0.015 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are special for V_{dd25} = 2.375 ÷ 2.625 V, V_{dd12}= 1.14 ÷ 1.26 and T = -40 ÷ +125 °C. Typical value are at V_{dd25}= 2.5V, V_{dd12}= 1.2V, T= 85 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Analog supply voltage	V_{dd25}	-	2.375	2.5	2.625	V
Digital supply voltage	V_{dd12}	-	1.14	1.2	1.26	V
Operating temperature range	T	-	-40	+85	+125	°C
Differential output voltage	V_{OD}	-	600	700	800	mV
Output offset voltage	V_{OS}	-	1.125	1.250	1.375	V
Change V_{OD}	ΔV_{OD}	-	-	-	50	mV
Change V_{OS}	ΔV_{OS}					
Differential time propagation delay, high to low	t_{PHLDT}	-	1	1.4	1.6	ns
Differential time propagation delay, low to high	t_{PLHDT}					
Line short circuit current	I_s	V_{PAD_OUTN} shorted to Vdd	-	3.5	-	mA
		V_{PAD_OUTN} shorted to ground	-	22	-	mA
Pair short circuit current	I_{sab}	V_{PAD_OUTP} shorted to V_{PAD_OUTN}	-	3.5	-	mA
Stand-by current	I_{st}	-	-	-	74	nA
Out current	I_{out}	IREF_TX = 10 uA	-	3.5	-	mA
		IREF_TX = 20 uA	-	7	-	mA
DC power current from V_{dd25}	I_{VDD25}	IREF_TX = 10 uA	6.2	6.5	6.8	mA
		IREF_TX = 20 uA	10.2	10.3	10.4	mA
Total power	P_{total}	IREF_TX = 10 uA	14.9	16.3	17.7	mW
		IREF_TX = 20 uA	24.5	25.8	27.3	mW
Rise time	t_{RT}	C_L=1p	330	340	350	ps
Fall time	t_{FT}		330	340	350	ps
AC power current from V_{dd25}	I_{VDD25}	IREF_TX = 10 uA	16.0	21.4	25.2	mA
AC power current from V_{dd}	I_{VDD}		0.35	0.35	0.37	mA
Total AC power	W		38.7	53.3	65.5	mW
Clock jitter, rms	t_{RJ}	C_L=1p	300	400	900	fs
Clock jitter, max (p-p)	t_{DJM}		0.8	1.3	6.0	ps
Data jitter, deterministic	t_{DJ}		0.8	1.3	6.0	ps
Duty cycle	S	-	49	50	51	%
Input voltage high level	V_{IH}	For digital inputs	$0.8V_{dd12}$	-	V_{dd12}	V
Input voltage low level	V_{IL}	For digital inputs	0	-	$0.2V_{dd12}$	V

Note: *$|V_{OD}|$=| V_{PAD_OUTP} - V_{PAD_OUTN} |
ΔV_{OD}=($|V_{OD}|$ for V_{PAD_OUTP} height and V_{PAD_OUTN} low) minus ($|V_{OD}|$ for V_{PAD_OUTP} low and V_{PAD_OUTN} height)
ΔV_{OS} =(V_{OS} for V_{PAD_OUTP} height and V_{PAD_OUTN} low) minus (V_{OS} for V_{PAD_OUTP} low and V_{PAD_OUTN} height)

8 TYPICAL CHARACTERISTICS

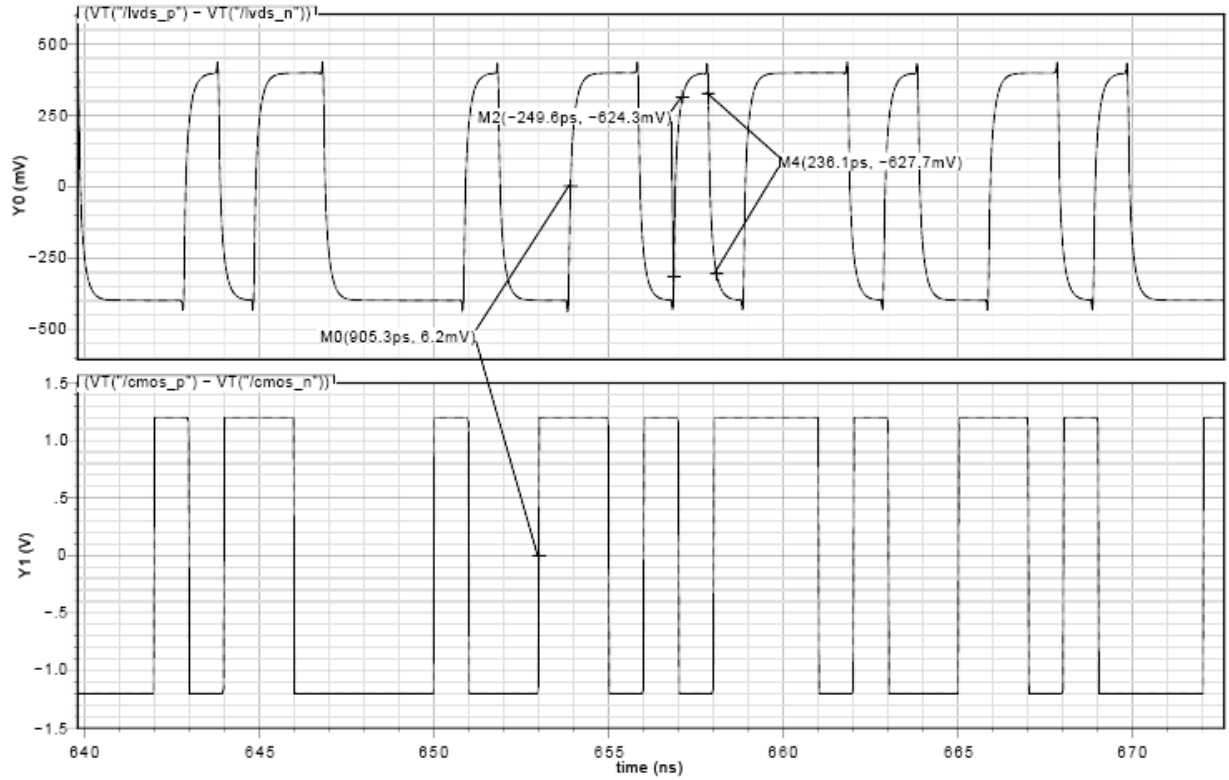

Figure 4: The time diagram of the transmitter at a frequency of 1 GHz.

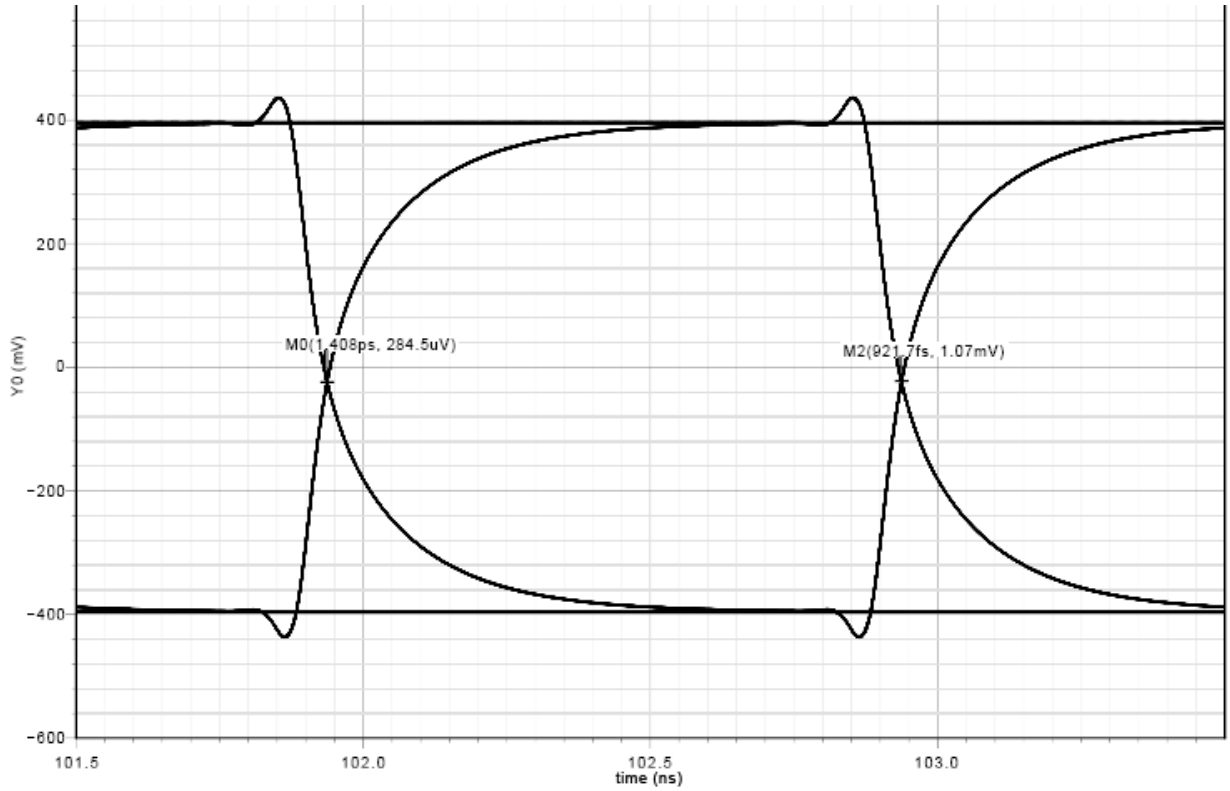

Figure 5: Transmitter “eye” diagram.

9 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation