2.4 Gbps LVDS transmitter

SPECIFICATION

1 FEATURES

- TSMC CMOS 0.065 um
- 2.5 V analog power supply
- 2.5 V CMOS input logic signals
- 2.4 Gbps (DDR MODE) switching rates
- Conforms to TIA/EIA-644 LVDS standards
- Temperature range: -40 °C to + 85 °C
- Optimized for pad-limited layout design
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- Point-to-point data transmission
- Multidrop buses
- Clock distribution
- Backplane data transmission
- Cable data transmission
- Half-duplex or duplex data transmission

3 OVERVIEW

The interface to the core logic includes differential signal pins (INP and INN) to transmit data, and two control pins (OEN and EN) to configure the state of the transmitter. There are other two internal pins (VREF and IREF) to get voltage reference and current reference. OUTP and OUTN are complementary outputs to connect to the bonding pads. LVDS transceiver cell may be used for half-duplex data transmission. In this case, input OEN controls the direction of the transmission. When OEN = 1, block operates in the receiver mode –the transmitter output is in high impedance state. When OEN = 0, block operates in the transmitter mode. In this case, the transmitter drives its output current into the differential LVDS line, with the polarity corresponding to the bit value being transmitted. This LVDS driver provides a high current mode (IREF equal 20uA or 19uA) for system designs that employ double termination (near-end and far-end) of the differential signaling lines. The low current drive mode (IREF equal 10uA or 9.5uA) is sufficient for typical single ended termination at the receiver.

4 STRUCTURE

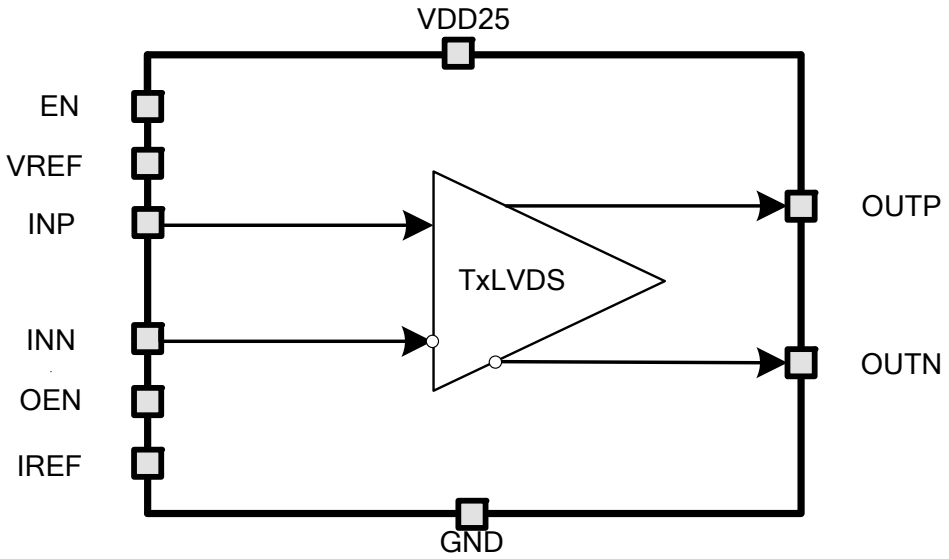

Figure 1: 2.4 Gbps LVDS transmitter structure.

5 PIN DESCRIPTION

Name	Direction	Description
IREF	IO	Reference current
VREF	I	Reference voltage 1.2V
OEN	I	Output enable pin, active low
EN	I	LVDS transmitter enable
INp	I	Input differential LVDS signal
INn		
OUTP	O	Output differential LVDS signal of transmitter
OUTN		
VDD25	IO	Supply voltage 2.5 V
GND	IO	Ground

Table 1: Truth table of LVDS transmitter.

Mode	Input				Output	
	EN	OEN	INP	INN	OUTP	OUTN
Transmit	1	0	0	1	0	1
			1	0	1	0
		1	X	X	Z	Z
Power down	0	X	X	X	Z	Z

6 LAYOUT DESCRIPTION

LVDS transmitter dimensions are given in the table 2.

Table 2: Block dimension.

Dimension	Value	Unit
Height	101	um
Width	145	um

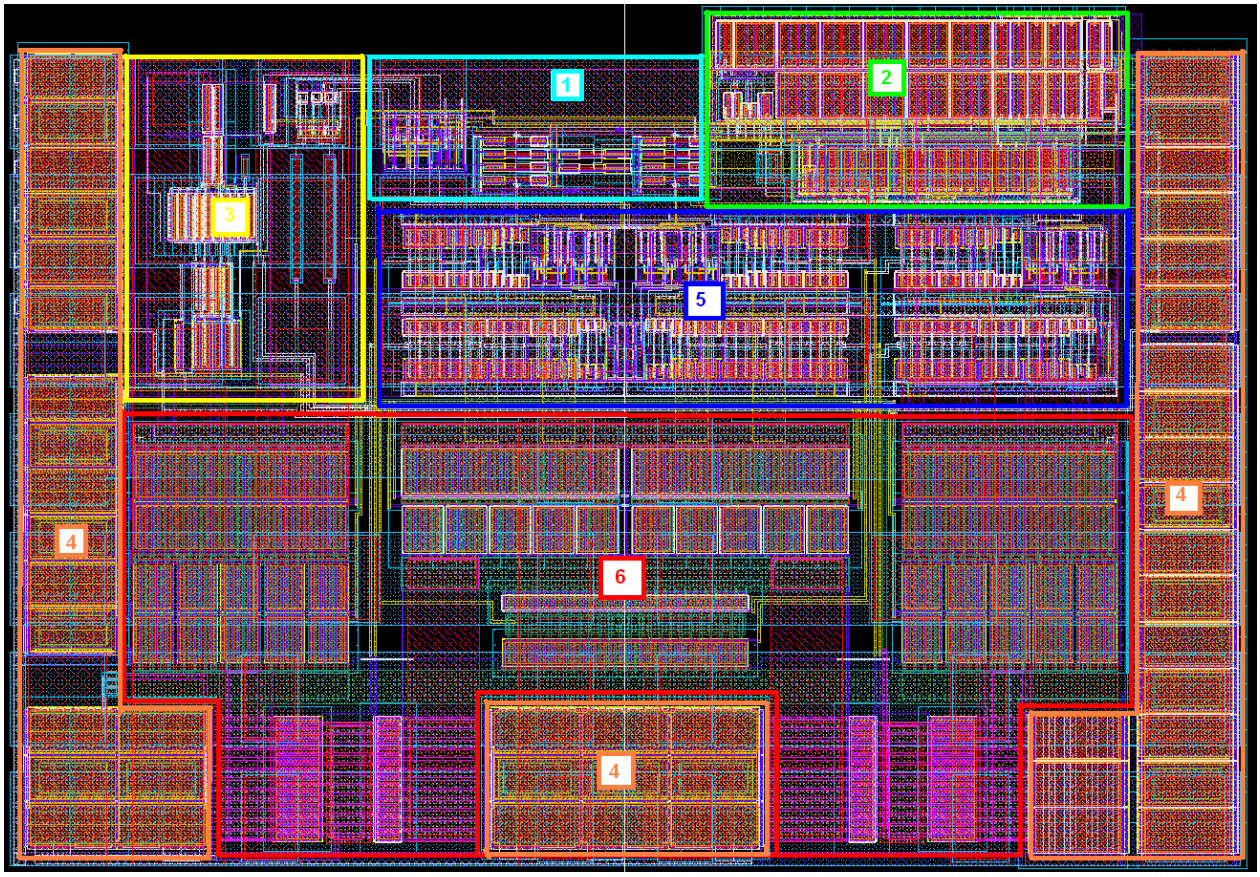

Figure 2: LVDS transmitter layout view.

1. Digital control
2. Bias
3. Common-mode regulator
4. MOS capacitors
5. Digital buffer
6. Output stage

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC 0.065um CMOS
Status _____ pre-silicon verification
Area _____ 0.015 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are special for V_{dd25} = 2.25 ÷ 2.75 V and T = -40 ÷ +85 °C. Typical value are at V_{dd25}= 2.5V, T=+27 °C, unless otherwise specified. For transmitter R_L=100±1% (load resistance), C_L- load capacitance, IREF=10uA.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Analog supply voltage	V_{dd25}	-	2.25	2.5	2.75	V
Operating temperature range	T	-	-45	+27	+85	°C
Differential output voltage	V_{OD}	IREF = 9.5 uA, R_L=100±1%	267	330	371	mV
		IREF = 10 uA, R_L=100±1%	282	350	390	mV
		IREF = 19 uA, R_L=50±1%	286	330	362	
		IREF = 20 uA, R_L=50±1%	302	350	380	
Output offset voltage	V_{OS}	(V_{OUTP} + V_{POUTN})/2	1.165	1.2	1.235	V
Differential time propagation delay, high to low	t_{PHL}	C_L=1p-	0.45	0.6	0.83	ns
Differential time propagation delay, low to high	t_{PLH}					
OEN to output enable (V_{OS})[1]	T_{OE}	C_L=1p-	0.67	1	1.5	ns
OEN to output disable (V_{OS})[2]	T_{OD}		0.87	1.2	1.6	ns
Differential skew between t_{PHL} and t_{PLH}	t_{skew1}		-	9	21	ps
Line short circuit current	I_{sa},I_{sb}	V_{OUTP} and V_{OUTN} shorted to ground	-	10.3	11.5	mA
Pair short circuit current	I_{sab}	V_{OUTP} shorted to V_{OUTN}	-	3.5	3.9	mA
Stand-by current	I_{st}	-	-	-	74	nA
DC power current from V_{dd25}	W_{DC}	IREF = 10 uA, R_L=100±1%	3.12	3.8	4.2	mA
		IREF = 20 uA, R_L=50±1%	6.61	7.6	8.3	mA
Total DC power	P_{total}	IREF = 10 uA, R_L=100±1%	7	9.5	11.5	mW
		IREF = 20 uA, R_L=50±1%	14.9	19	22.8	mW
Rise time	t_{RT}	C_L=1p	60	71	94	ps
Fall time	t_{FT}		60	71	94	ps
AC power current from V_{dd25}	I_{VDD25}	IREF = 10 uA	8.7	9.9	11.2	mA
Total AC power	W_{AC}		19.6	24.7	30.8	mW
Clock jitter, rms	t_{RJ}	C_L=1p	40	63	110	fs
Clock jitter, max (p-p)	t_{DJM}		0.25	0.4	0.68	ps
Data jitter, deterministic	t_{DJ}		0.3-	0.4	1	ps
Data jitter, deterministic crossing ±100mV	t_{DJC}		26	27	28	ps
Data jitter, deterministic	t_{DJ}	C_L=3p	9	10	11	ps
Data jitter, deterministic crossing ±100mV	t_{DJC}		95	95	112	ps
Duty cycle	S	-	49	50	51	%
Input voltage high level	V_{IH}	For digital inputs	0.8V_{dd12}	-	V_{dd12}	V
Input voltage low level	V_{IL}	For digital inputs	0	-	0.2V_{dd12}	V

Note: *|V_{OD}|=| V_{OUTP} - V_{POUTN} |
[1] Output recovery to voltage within the offset voltage range
[2] Output drops out of the output offset voltage range

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation