Rail to Rail LVDS receiver 2 Gbps

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- 1.2 V CMOS input and output logic signals
- 2 Gbps (DDR MODE) switching rates
- Conforms to TIA and IEEE standards without hysteresis
- Rail to rail input range
- Optimized for pad-limited layout design
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- Point-to-point data receiver
- Multidrop buses
- Clock distribution
- Backplane receiver
- Backplane data receiver
- Cable data receiver

3 OVERVIEW

LVDS_RX is LVDS receiver with rail to rail input range. EN_T enables 100 Ohm internal resistor. The CAL_T<1:0> adjusts 100 Ohm internal resistor, the design target is to compensate the resistance deviation. The VREF12 is input 1.2 V voltage reference. Pin IREF_RX to get current 20 uA reference from receiver bias. INP and INN are complementary input to connect to the bonding pads. This LVDS receiver does not employ hysteresis, and therefore does not comply with the hysteresis requirement of the TIA and IEEE standards for LVDS differential signaling at the specified rates.
The block is designed on TSMC CMOS 65 nm technology.

4 STRUCTURE

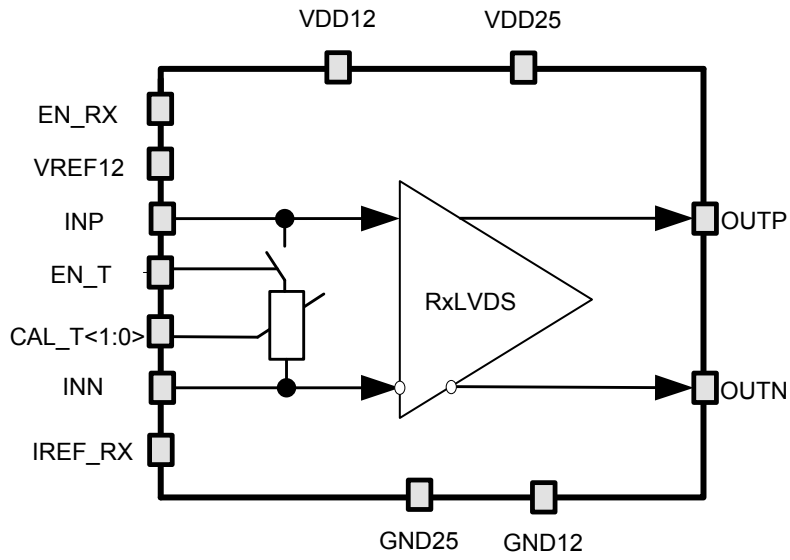

Figure 1: LVDS structure

5 PIN DESCRIPTION

Name	Direction	Description
IREF_RX	I	Reference current 20 uA
VREF12	I	Reference voltage 1.2 V
EN_T	I	On-chip resistor enable
CAL_T<1:0>	I	On-chip resistor value adjust
EN_RX	I	LVDS receiver enable
INP	I	Input differential LVDS signal
INN		
OUTP	O	Output differential 1.2 V CMOS signal
OUTN		
VDD12	IO	Supply voltage 1.2 V
VDD25	IO	Supply voltage 2.5 V
GND25	IO	Analog ground
GND12	IO	Digital ground

Table 1: LVDS receiver truth table

Mode	Input			Output	
	EN_RX	PAD_INP	PAD_INN	OUTp	OUTn
Receive	1	1	0	1	0
		0	1	0	1
Power down	0	X	X	1	0

Table 2: Input 100 Ohm resistor compensation

Input		On-Chip 100Ohm Resistor compensation
RES_CAL<1>	RES_CAL<0>	
0	0	-10 %
0	1	0 %
1	0	0 %
1	1	+10 %

6 LAYOUT DESRIPTION

Rail to Rail LVDS dimensions are given in the table 3.

Table 3: Block dimension

Dimension	Value	Unit
Height	210	um
Width	235	um

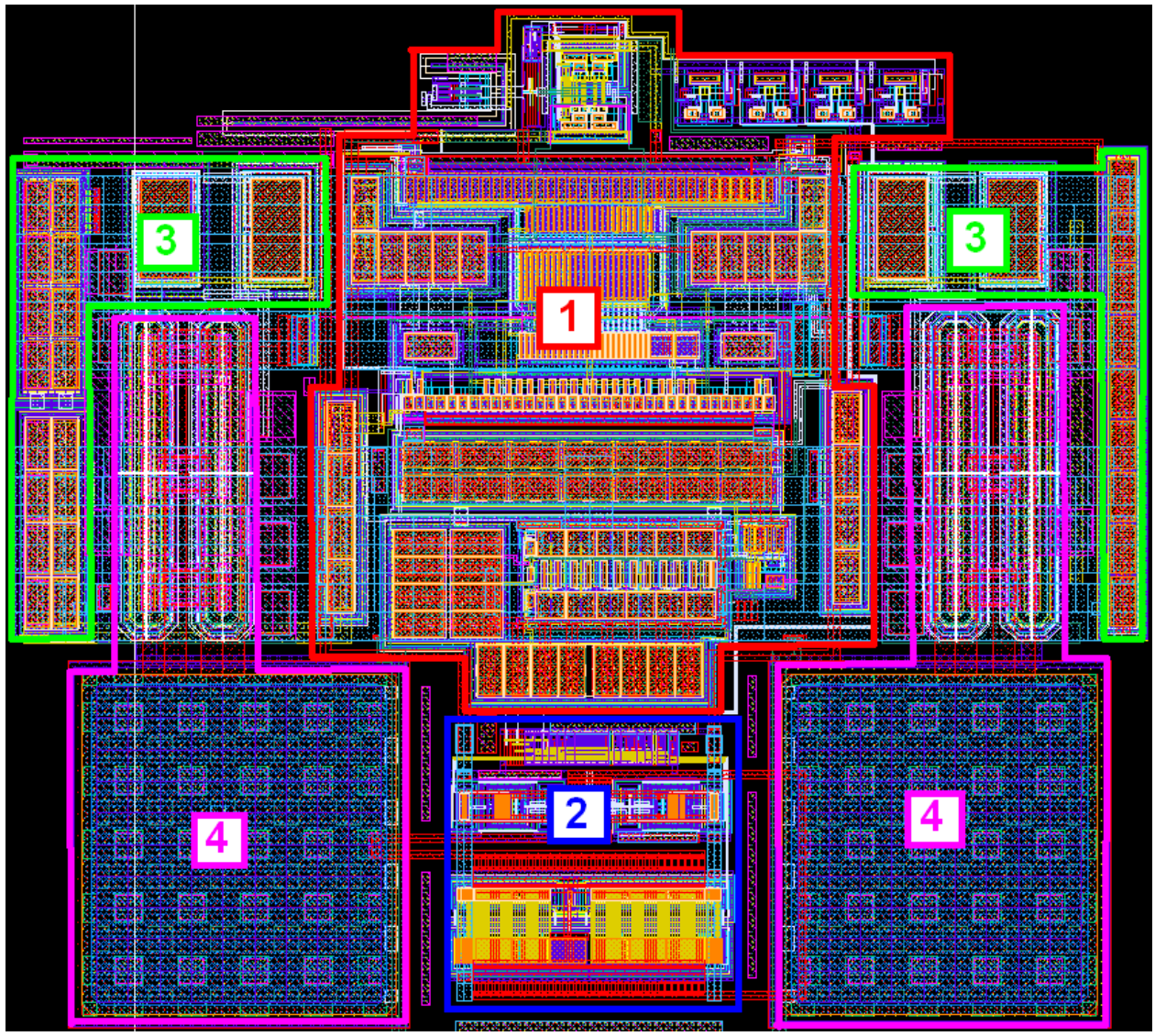

Figure 2: Rail to rail LVDS Receiver with pads layout

1. Rail to rail LVDS receiver
2. Input 100 Ohm resistor
3. Capacitance
4. Pads

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC CMOS 65 nm
Status _____ silicon proven
Area _____ 0.049 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are special for V_{dd25} = 2.25 ÷ 2.75 V, V_{dd12}= 1.08÷ 1.32 V, T_j = -40 ÷ +85 °C. Typical value are at V_{dd25}= 2.5 V, V_{dd12}= 1.2 V, T_j=+ 27 °C, V_{id}=|V_{INP}-V_{INN}|=100 mV unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply analog voltage	V_{dd25}	-	2.25	2.5	2.75	V
Supply digital voltage	V_{dd12}	-	1.08	1.2	1.32	V
Operating temperature range	T_j	-	-40	27	+85	°C
Input current range	I_{in}	EN_T= “1”	-	-	10	mA
Input voltage range	V_{in}	-	0	1.2	2.4	V
Input differential threshold	V_{th}	-	-	-	100	mV
Receiver differential input impedance	R_{in}	With calibration	90	100	110	Ω
		Without calibration T_CAL<1:0>= “10” or T_CAL<1:0>= “01”	83	100	120	
		Without calibration T_CAL<1:0>= “11”	90	109	130	
DC power current from V_{dd25}	I_{VDD25}	-	1.9	2.06	2.3	mA
DC total power	P_{total}		4.3	5.1	6.3	mW
Stand-by current	I_{st_vdd25}	-	12	21	98	nA
Stand-by current	I_{st_vdd12}	-	1	1.7	257	nA
Output voltage range	V_{out}	-	0	-	1.2	V
Differential propagation delay, high to low	t_{PHLDT}	-	453	587	872	ps
Differential propagation delay, low to high	t_{PLHDT}	-	453	587	873	ps
Average current from V_{dd25}	I_{VDD25}	F_{clk}=1 GHz	2.26	2.5	2.83	mA
Average current from V_{dd12}	I_{VDD12}		78	89	103	uA
Total average power	W		5.2	6.3	7.9	mW
Deterministic jitter, peak-to-peak	t_{DJ}	2 Gbps	-	8.8	31	ps
		1.8 Gbps	-	6.8	13.3	ps
		1.6 Gbps	-	6.1	7.6	ps
Random jitter, rms	t_{RJ}	V_{id}=100 mV, F_{clk}=1 GHz	312	413	973	fs
Random jitter, max (p-p)	t_{DJM}		4.4	5.8	13.6	ps
Random jitter, rms	t_{RJ}	V_{id}=250 mV, F_{clk}=1 GHz	154	194	388	fs
Random jitter, max (p-p)	t_{DJM}		2.1	2.7	5.4	ps
Input voltage high level	V_{IH}	For digital inputs	0.8 V_{dd12}	-	V_{dd12}	V
Input voltage low level	V_{IL}		0	-	0.2 V_{dd12}	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Layout or blackbox
- Verilog, lef and lib files
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation