Programmable CMOS LVDS Transmitter/Receiver

SPECIFICATION

1. FEATURES

- Technology TSMC 0.13um CMOS
- 3.3 V analog power supply
- 1.2 V digital power supply
- 1.2V CMOS input and output logic signals
- 8-step (3-bit) adjustable transmitter output current (range from 0.75mA to 6.5mA)
- 1.25 Gbps (DDR MODE) switching rates
- Conforms to TIA/EIA-644 LVDS standards without hysteresis
- Two receiver cell types: rail to rail and reduced input range
- Temperature range: -40 °C to + 125 °C
- Optimized for pad-limited layout design
- Portable to other technologies (upon request)

2. APPLICATION

- Point-to-point data transmission
- Multidrop buses
- Clock distribution
- Backplane receiver
- Backplane data transmission
- Cable data transmission

3. OVERVIEW

LVDS device consists of one common bandgap reference voltage generator, a number of LVDS transmitter pad groups with their bias blocks, and a number of LVDS receiver pad groups (whether rail to rail or reduced input range) with their bias blocks. Also, LVDS transceiver pad groups may be used. In this case, the receiver bias and the transmitter bias blocks should be instantiated for each transceiver pad group. Group size is defined by the corresponding bias output dimension. In the case when desired group size is not the power of 2, several bias blocks should be used, or bias block with size larger than the group size can be instantiated. For example (see fig 1.), to create 6 RX LVDS lines and 30 TX LVDS lines, one LVDSBIASRX4X, one LVDSBIASRX2X, and one LVDSBIASTX32X cells can be instantiated. Two current lines of the LVDSBIASTX32X cell (that are not connected to the LVDS TX pads) should be left open. For the layout design, it is recommended to place bias blocks as close as possible to their corresponding receiver, transmitter, or transceiver pads. It should be noted that all pad cell ground pins in a group, and the corresponding bias block ground pin should be connected together. However, bandgap reference block ground may be connected to the different ground net, as well as different pad groups may utilize different ground nets.

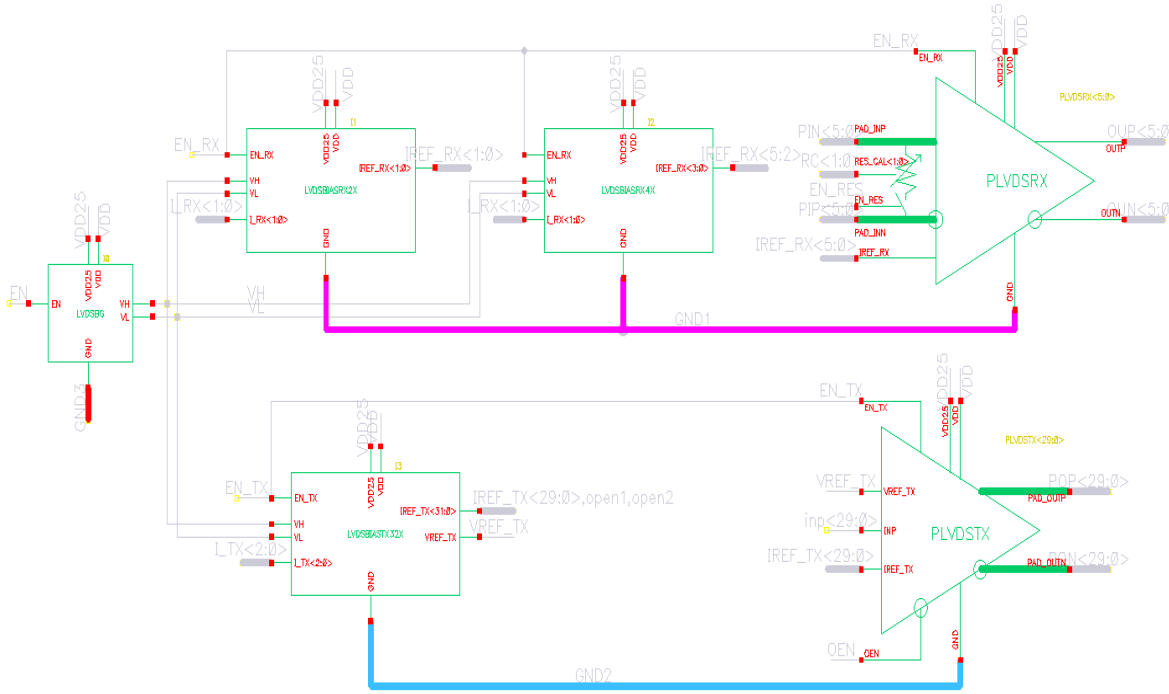

Figure 1: Schematic of LVDS connection example.

LVDS transmitter (cell PLVDSTX) comprises current source with nominal value 3.5 mA, and output voltage regulator, which holds 1.25V DC common mode output voltage. Output current changes its polarity depending on the data being transmitted. Transmitter output current may be adjusted by setting bits I_TX<2:0> of the corresponding transmitter bias block, while the nominal value of 3.5 mA corresponds to the bit code “100”. Thus, output current adjustment is made for all the transmitter pads in a group. LVDS transmitter output may be switched into high-impedance state by setting high input OEN.

LVDS receiver cells (PLVDSRX and PLVDSRXL) comprise a voltage comparator with input connected to the 100-Ohm termination resistor. As the comparator has high input impedance, most of the input current flows through the termination resistor, producing a voltage drop of 350 mV typically. Voltage polarity across the resistor changes depending on the input current direction. Comparator circuit converts the voltage drop polarity into the corresponding logical value of the 1.2V CMOS output signals. Receiver with reduced input range (cell PLVDSRXL) has smaller size and current consumption than the receiver with rail-to-rail input range (cell PLVDSRX). In the case when the receiver and the transmitter have low impedance common ground connection (no significant voltage mismatch between the receiver and the transmitter ground), the usage of the receiver with reduced input range is preferred. Receiver comparator reference current may be adjusted by setting bits I_RX<1:0> of the corresponding receiver bias block. Normally these bits should be set to their default value “10”. In the case when receiver accuracy requirements are not strict (for example, when the input signal frequency is low) the comparator reference current may be set lower, in order to reduce the receiver current consumption. Receiver pad cell also comprises internal termination resistor with adjustable value. Input bits RES_CAL<1:0> are used for adjusting the termination resistance. The design target is to compensate 100 ohm resistance deviation from 20% to 10%. In order to use an external termination, the internal resistor may be switched off by setting low input RES_EN.

LVDS transceiver cell may be used for half-duplex data transmission. In this case, input OEN controls the direction of the transmission. When OEN = 1, block operates in the receiver mode – the input termination resistor is on (when enabled by RES_EN), and the transmitter output is in high impedance state. When OEN = 0, block operates in the transmitter mode. In this case, the transmitter drives its output current into the differential LVDS line, with the polarity corresponding to the bit value being transmitted.
All LVDS library blocks are designed in the TSMS CMOS 130 nm process. 130TSMC_LVDS_04 LVDS IO library is preferred to use in pad-limited layout design because all common part of transmitters and receivers combined in cells which placed inside core of die and only driver of transmitters and comparator of receivers are placed inside pad ring. All LVDS blocks layouts are delivered separately.

4. LIBRARY STRUCTURE

Table 1 shows the cell category including cell name and their descriptions. LVDS I/O library includes transmitter, two receivers, bidirectional cell, set of bias for receiver, set of bias for transmitter and bandgap voltage reference.

Table 1: Cell Category.

Cell name	**Description**
LVDSBG	Bandgap voltage reference
LVDSBIASRXnX	LVDS bias for receiver, n=1,2,4,8,16,32 is the number of output currents
LVDSBIASTXnX	LVDS bias for transmitter, n=1,2,4,8,16,32 is the number of output currents
PLVDSTX	LVDS transmitter PAD cell
PLVDSRX	LVDS rail to rail input range receiver PAD cell
PLVDSRXL	LVDS reduced input range receiver PAD cell
PLVDSRXTX	LVDS transceiver PAD cell

5. LAYOUT DESCRIPTION

The cell dimensions are given in the table 2

Table 2: Cell dimensions

Cell Name	**Cell Width (um)**	**Cell Heigh (um)**	**Cell Area (um^2)**	**Location**	**Bonding Pad No.**
PLVDSTX	120	190	22800	Pad ring	2
PLVDSRX	180	190	34200	Pad ring	2
PLVDSRXL	160	190	30400	Pad ring	2
PLVDSRXTX	300	190	57000	Pad ring	2

6. OPERATING CHARACTERISTICS

6.1 TECHNICAL CHARACTERISTICS

Technology TSMC 0.13um CMOS
Status pre-silicon verification

6.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are special for VDD33= 2.97 ÷ 3.63 V, VDD= 1.08 ÷ 1.32 and T = -40 ÷ +125 °C. 1.25Gbps - switching (625MHz). For transmitter R_{Load}=100±1%. C_L- load capacitance.
Typical value are at VDD33= 3.3V, VDD= 1.2V, T=+ 27 °C unless otherwise specified.
All parameters of receivers and transmitters measure full schematic, i.e with bandgap voltage reference and biases.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply analog voltage	VDD33	-	2.97	3.3	3.63	V
Supply digital voltage	VDD	-	1.08	1.2	1.32	V
Operating temperature range	T	-	-40	+27	+125	°C
Differential output voltage	V_{OD}	PLVDSTX, PLVDSRXTX in transmission mode	285	355	465	mV
Output offset voltage	V_{OS}		1.184	1.25	1.275	V
Output voltage high, V_{PAD_OUTP} or V_{PAD_OUTN}	V_{Oh}		-	-	1.507	V
Output voltage low, V_{PAD_OUTP} or V_{PAD_OUTN}	V_{Ol}		1.009	-	-	V
|Change V_{OD}|	ΔV_{OD}		-	-	50	mV
|Change V_{OS} |	ΔV_{OS}		-	-	50	mV
Out current	I_{out}		2.846	3.547	4.651	mA
DC power current from VDD33	I_{VDD33}	PLVDSTX	2.988	3.722	4.882	mA
DC power current from VDD33	I_{VDD33}	PLVDSRXTX in transmission mode	4.15	5.183	6.817	mA
Input impedance	Z_{in}	PLVDSRX, PLVDSRXL, PLVDSRXTX in receive mode	90	100	110	Ω
Input differential threshold	V_{th}		-	-	100	mV
Input voltage range (common-mode)	V_{in}	PLVDSRX, PLVDSRXTX in receive mode	0	1.25	3.3	V
Input voltage range (common-mode)	V_{in}	PLVDSRXL	0	1.25	1.9	V
DC power current from VDD33	I_{VDD33}	PLVDSRX	1.146	1.442	1.929	mA
DC power current from VDD33	I_{VDD33}	PLVDSRXL	0.477	0.598	0.786	mA
DC power current from VDD	I_{VDD}		0.328	0.441	0.602	mA
Differential time propagation delay, high to low	t_{PHLDT}	PLVDSTX	1.4	2.0	3.2	ns
Differential time propagation delay, low to high	t_{PLHDT}		1.4	2.0	3.2	ns
Rise time	t_{RT}	20% to 80% PLVDSTX	65.7	89.1	130.2	ps
Fall time	t_{FT}		65.9	88.8	130.1	ps
Clock jitter, random rms	tRJ		199	312	918	fs
Clock jitter, random max (p-p)	tDJM		1.128	1.474	5.007	ps
Data jitter, deterministic	tDJ		0.9	2.6	30.7	ps
Differential time propagation delay, high to low	tPHLDT		1.4	2.0	3.2	ns

Table electrical characteristics (continue)

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Differential time propagation delay, low to high	t_{PLHDT}		1.4	2.0	3.2	ns
Rise time	t_{RT}	20% to 80% PLVDSTXRX, transmit mode	181	190	219	ps
Fall time	t_{FT}		177	192	225	ps
Clock jitter, random rms	t_{RJ}	C_L=3p PLVDSTXRX, transmit mode	204	348	1015	fs
Clock jitter, random max (p-p)	t_{DJM}		1.158	1.72	5.3	ps
Data jitter, deterministic	t_{DJ}		9.23	13.8	45	ps
Differential time propagation delay, high to low	t_{PHLDT}	C_L=100f PLVDSRX	0.707	0.886	1.339	ns
Differential time propagation delay, low to high	t_{PLHDT}		0.707	0.885	1.338	ns
Clock jitter, random rms	t_{RJ}		334	641	1142	fs
Clock jitter, random max (p-p)	t_{DJM}		1.77	2.89	4.74	ps
Data jitter, deterministic	t_{DJ}		0.8	2.75	33.75	ps
Differential time propagation delay, high to low	t_{PHLDT}	C_L=100f, PLVDSRXL	0.472	0.639	0.996	ns
Differential time propagation delay, low to high	t_{PLHDT}		0.471	0.638	0.997	ns
Clock jitter, random rms	t_{RJ}		487	633	1254	fs
Clock jitter, random max (p-p)	t_{DJM}		1.893	3.43	7.71	ps
Data jitter, deterministic	t_{DJ}		0.9	1	6.9	ps
Differential time propagation delay, high to low	t_{PHLDT}	C_L=100f, PLVDSTXRX, receive mode	0.622	0.868	1.325	ns
Differential time propagation delay, low to high	t_{PLHDT}		0.622	0.867	1.323	ns
Clock jitter, random rms	t_{RJ}		404	525	1166	fs
Clock jitter, random max (p-p)	t_{DJM}		1.9	2.8	5.9	ps
Data jitter, deterministic	t_{DJ}		0.9	2.64	32	ps
Input voltage high level	V_{IH}	For digital inputs	0.8VDD	-	VDD	V
Input voltage low level	V_{IL}		0	-	0.2 VDD	V

$|V_{OD}|=| V_{PAD\_OUTP} - V_{PAD\_OUTN} |$

ΔV_{OD}=($|V_{OD}|$ for V_{PAD_OUTP} height and V_{PAD_OUTN} low) minus ($|V_{OD}|$ for V_{PAD_OUTP} low and V_{PAD_OUTN} height)

ΔV_{OS} =(V_{OS} for V_{PAD_OUTP} height and V_{PAD_OUTN} low) minus (V_{OS} for V_{PAD_OUTP} low and V_{PAD_OUTN} height)

7. DELIVERABLES

LVDS IO library supports different popular EDA tools to integrate it with other libraries and IPs.

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation