1 Gbps LVDS transmitter

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.13 um
- 3.3 V power supply
- 1 Gbps (DDR MODE) switching rates
- Conforms to TIA/EIA-644 LVDS standards
- Temperature range: -40 °C to + 85 °C
- Optimized for pad-limited layout design
- Portable to other technologies (upon request)

2 APPLICATION

- Point-to-point data transmission
- Multidrop buses
- Clock distribution
- Backplane data transmission
- Cable data transmission
- Half-duplex or duplex data transmission

3 OVERVIEW

The LVDS transmitter converts CMOS data to LVDS data stream. It could transmit data or clock signals with rate up to 1 Gbps DDR MODE. LVDS transmitter corresponds to TIA/EIA-644 LVDS standards.
The LVDS transmitter is designed on iHP SiGe BiCMOS 0.13 um technology.

4 STRUCTURE

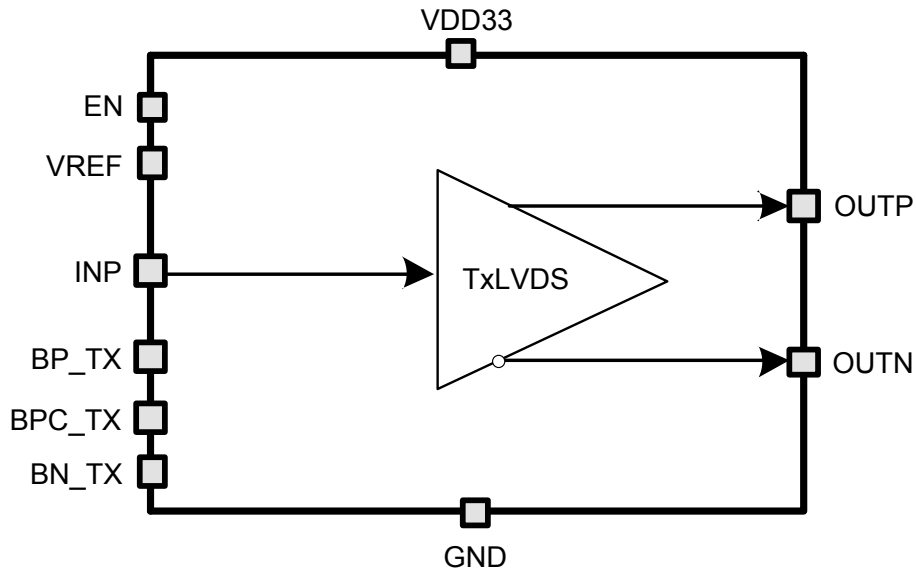

Figure 1: 1 Gbps LVDS transmitter structure.

5 PIN DESCRIPTION

Name	Direction	Description
BP_RX	I	Voltage reference from bias
BPC_RX		
BN_RX		
VREF	I	Reference voltage 1.2V
EN	I	LVDS transmitter enable
INP	I	Input CMOS signal
OUTP	O	Output differential LVDS signal of transmitter
OUTN		
VDD	IO	Supply voltage 3.3 V
GND	IO	Ground

Table 1: Truth table of LVDS transmitter

Mode	Input		Output	
	EN	INP	OUTP	OUTN
Transmit	1	0	0	1
		1	1	0
Power down	0	X	Z	Z

6 LAYOUT DESCRIPTION

LVDS transmitter dimensions are given in the table 2.

Table 2: Block dimension.

Dimension	Value	Unit
Height	98	um
Width	201	um

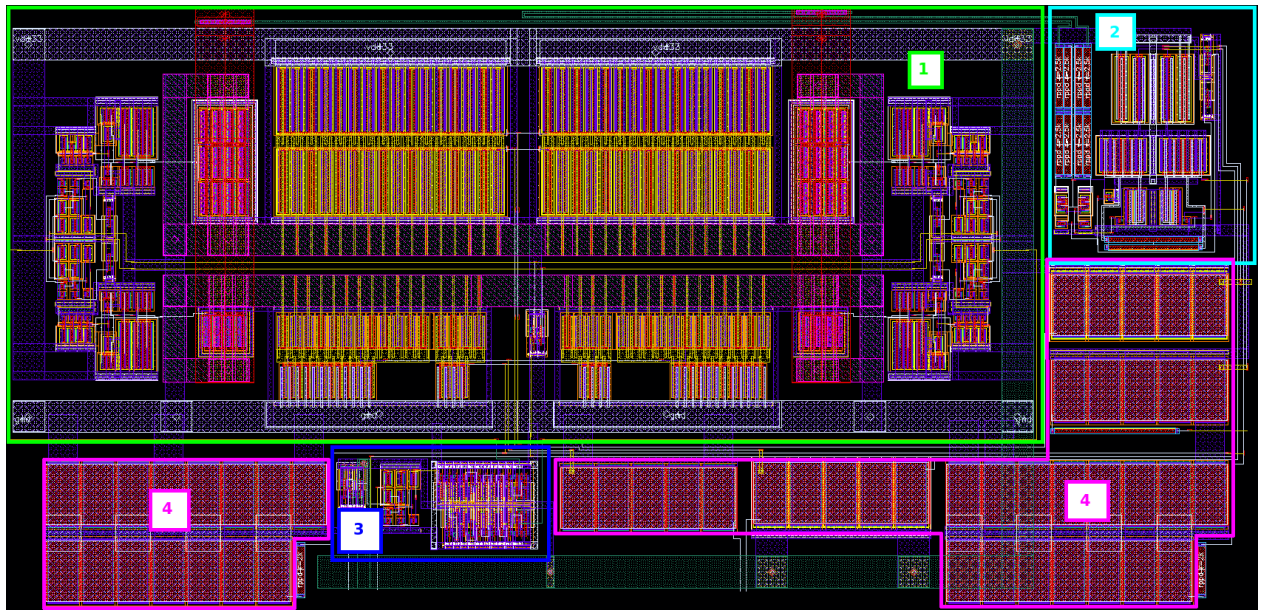

Figure 2: LVDS transmitter layout view.

1. Output stage
2. Common-mode regulator
3. Digital logic
4. MOS capacitors

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ SiGe BiCMOS 0.13um
Status _____ pre-silicon verification
Area _____ 0.02 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are special for V_{dd} = 2.7 ÷ 3.6 V and T = -40 ÷ +85 °C. Typical value are at V_{dd}= 3.3, T=27 °C, unless otherwise specified. For transmitter R_L=100±1% (load resistance), C_L- load capacitance.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Analog supply voltage	V_{dd}	-	2.7	3.3	3.6	V
Operating temperature range	T	-	-40	27	+85	°C
Differential output voltage	V_{OD}	$\|V_{OD}\|=\|V_{OUTP} - V_{OUTN}\|$	250	320	400	mV
Output offset voltage	V_{OS}	$\|V_{OUTP} + V_{OUTN}\|/2$	1.125	1.2	1.275	V
Differential time propagation delay, high to low	t_{PHL}	C_L=1p	1.4	1.76	2.9	ns
Differential time propagation delay, low to high	t_{PLH}					
Differential skew between t_{PHL} and t_{PLH}	t_{skew1}	-	-	13	14.5	ps
Line short circuit current	I_{sa},I_{sb}	V_{OUTP} and V_{OUTN} shorted to ground	3.15	3.17	3.18	mA
Pair short circuit current	I_{sab}	V_{OUTP} shorted to V_{OUTN}	3.15	3.17	3.18	mA
Stand-by current	I_{st}	-	0.6	0.8	14.4	nA
DC power current from V_{dd}	I_{DC}	-	3.34	3.37	3.38	mA
Total DC power	W_{DC}	-	9	11	12.2	mW
AC power current from V_{dd}	I_{VDD}	-	5.35	6	6.4	mA
Total AC power	W_{AC}	-	14.4	19.8	23	mW
Rise time	t_{RT}	C_L=1p	81	86	103	ps
Fall time	t_{FT}		84	89	106	ps
Clock jitter, rms	t_{RJ}	C_L=1p	140	230	500	fs
Clock jitter, max (p-p)	t_{DJM}		0.8	1.56	2.87	ps
Data jitter, deterministic	t_{DJ}		0.5	1.4	4	ps
Data jitter, deterministic crossing ±100mV	t_{DJC}		37	38	47	ps
Duty cycle	S	-	49	50	51	%
Input voltage high level	V_{IH}	For digital inputs	0.8V_{dd}	-	V_{dd}	V
Input voltage low level	V_{IL}		0	-	0.2V_{dd}	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.1:

- Section 3
- Subsection 7.2 update