1.2 Gbps LVDS transmitter/receiver

SPECIFICATION

1 FEATURES

- TSMC CMOS 180 nm
- 3.3 V power supply
- 1.2 Gbps (DDR MODE) switching rates (600 MHz)
- Half-duplex or full-duplex operation mode
- Conforms to TIA/EIA-644 LVDS standards without hysteresis
- Temperature range: -60 °C to + 100 °C
- Optimized for pad-limited layout design
- Portable to other technologies (upon request)

2 APPLICATIONS

- Point-to-point data receiver
- Point-to-point data transmission
- Multidrop buses
- Clock distribution
- Backplane data receiver
- Backplane data transmission
- Cable data receiver
- Cable data transmission

3 OVERVIEW

Core logic interface in receiver part includes complementary signal pins (**out_p** and **out_n**) for data transmission and control pins (**en_rx**, **ten**, **t_cal<1:0>**, **oen**) for receiver configuration. Core logic interface in transmitter part includes complementary signal pins (**in_p** and **in_n**) for data transmission and control pins (**en_tx, x2i**) for transmitter configuration. Internal analog pins **vref12**, **iref_20u_tx**, **iref_20u_rx** are reference voltage and currents inputs. Bi-directional differential pins **IOP** and **ION** should be connected to bonding pads.
The block may operate as LVDS receiver, transmitter or half-duplex transceiver.
The latter one is selected by setting both **en_tx** and **en_rx** controls to '1'. In this case port direction is toggled by **oen** control ('1' - RX, '0' - TX). In RX mode transmitter output is switched to high-impedance state, while in TX mode internal termination is disabled.
In single-direction applications configuration should be selected by **en_tx**, **en_rx** pins in order to save power. Double output current option (**x2i**=1) is included for dual termination designs – near-end and far-end. Internal termination is switched on by **ten** control and it's value may be calibrated from 20% to 10% deviation using **t_cal<1:0>** parameter.
The block is designed on TSMC 180 nm CMOS technology.

4 STRUCTURE

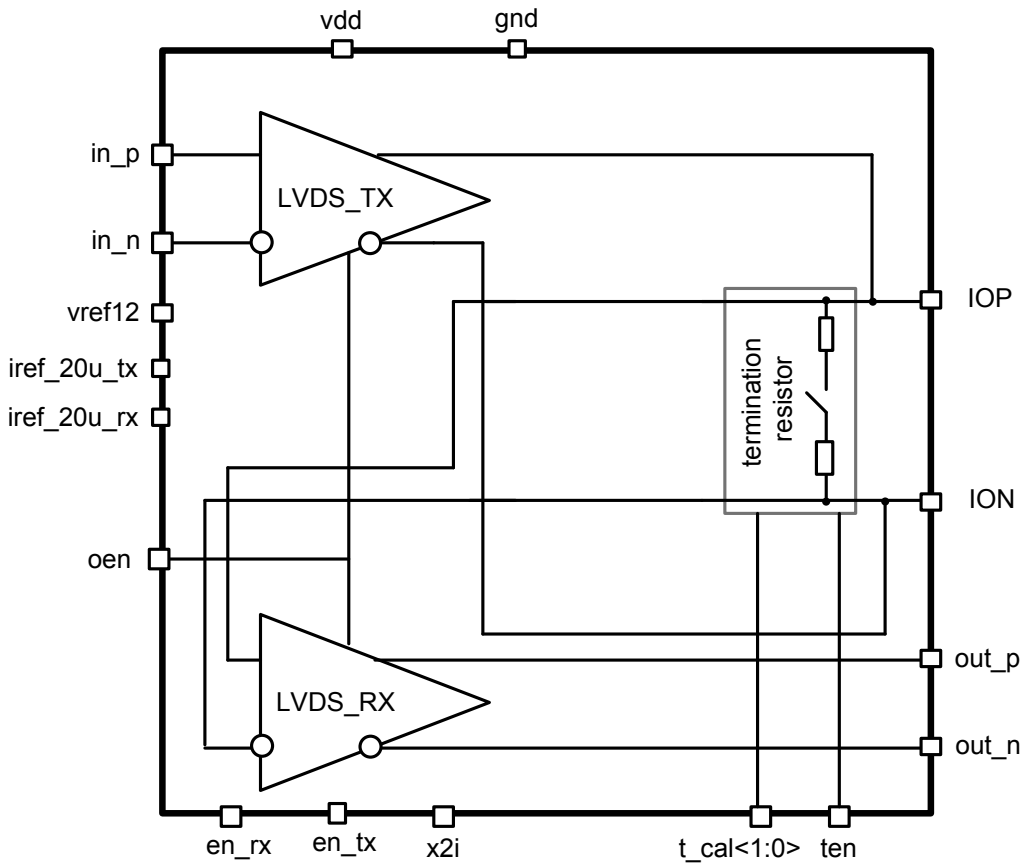

Figure 1: Functional block diagram

5 PIN DESCRIPTION

Name	Direction	Description
iref_20u_tx	IO	Reference current (20 uA) for transmitter
iref_20u_rx	IO	Reference current (20 uA) for receiver
vrev12	I	Reference voltage 1.2 V
en_tx	I	Transmitter enable
en_rx	I	Receiver enable
oen	I	receive or transmitter mode
x2i	I	Double output current for transmitter enable
t_cal<1:0>	I	On-chip resistor value adjust pins
ten	I	On-chip resistor enable
in_p	I	Transmitter CMOS complementary data inputs
in_n		
out_p	O	Receiver CMOS complementary data outputs
out_n		
IOP	IO	Bidirectional differential LVDS signal
ION		
vdd	IO	Supply voltage 3.3 V
gnd	IO	Ground

Table 1: Input 100 Ohm resistor compensation.

Input		On-Chip 100 Ohm Resistor compensation
t_cal<1>	t_cal <0>	
0	0	-8.8 %
0	1	0 %
1	0	0 %
1	1	+7.4 %

Table 2: Truth table of LVDS transmitter/receiver.

Mode	Input					Output		Input/Output	
	en_tx	en_rx	oen	in_p	in_n	out_p	out_n	IOP	ION
Transmitter	1	0	X	1	0	1	0	1	0
				0	1			0	1
Receiver	0	1		X	X	1	0	1	0
						0	1	0	1
Transmitter half-duplex mode	1	1	0	1	0	1	0	1	0
				0	1			0	1
Receiver half-duplex mode			1	X	X	1	0	1	0
						0	1	0	1
Power down	0	0	X	X	X	1	0	Z	Z

Here and below “Z” stands for “high impedance” and “X” means “don’t care”.

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 3.

Table 3: Block dimensions.

Dimension	Value	Unit
Height	250	um
Width	240	um

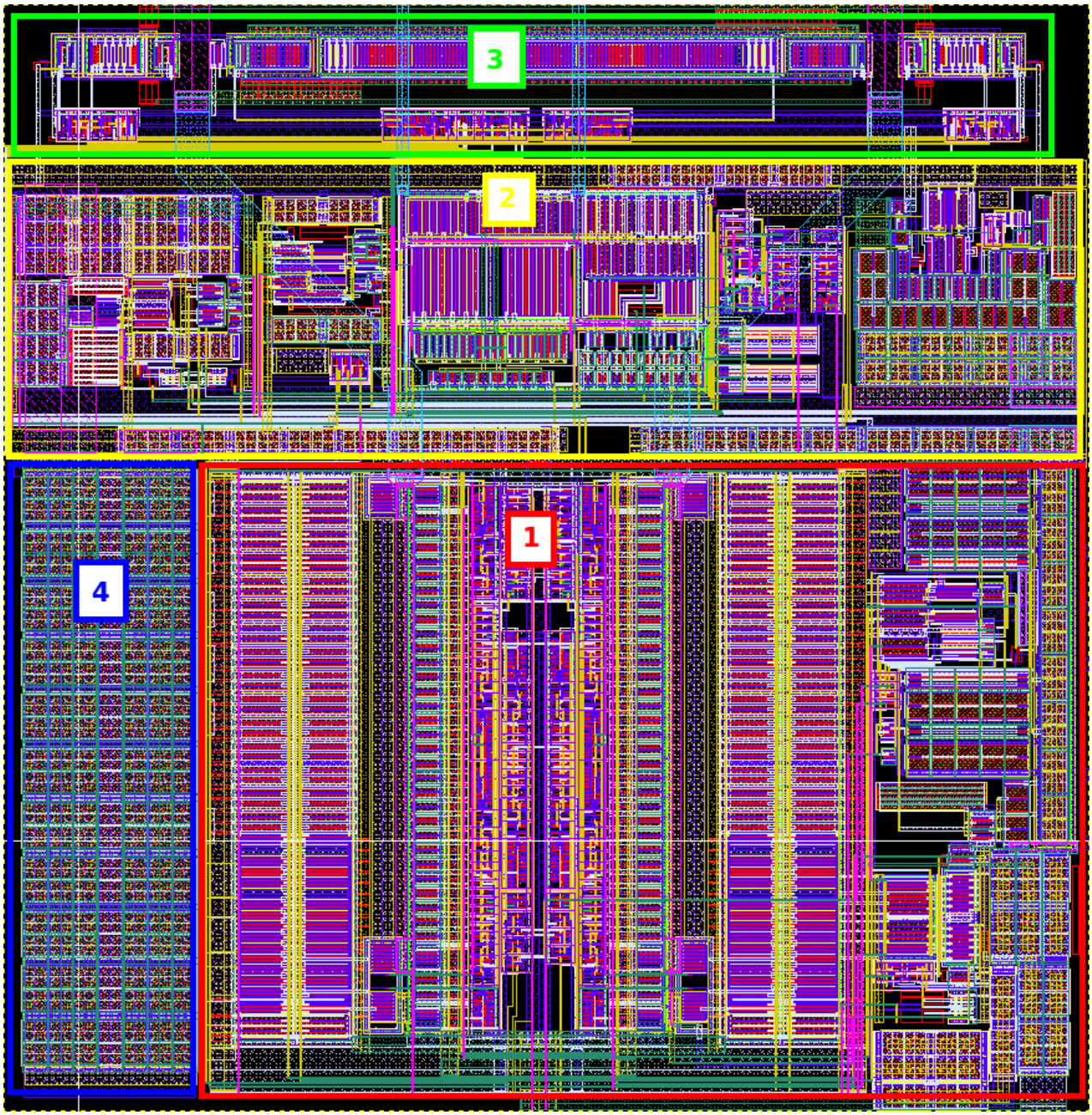

Figure 2: Device layout view.

1. Transmitter
2. Receiver
3. On-chip resistor
4. MOS capacitors

7 OPERATION CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS 180 nm
Status pre-silicon verification
Area 0.06 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{dd\_}$ = 3.0÷3.6 V and T = -60 ÷ +125 °°C. Typical values are at V_{dd} = 3.3V and T = 27° C, unless otherwise specified. For AC analyze 1.2 Gbps switching (600 MHz). For transmitter R_{Load}=100±1% (load resistance between nodes IOP and ION). V_{ind}- differential input voltage receiver (V_{IOP}- V_{ION}), C_{LTX}- load capacitance (capacitance on nodes IOP and ION), C_{LRX}- load capacitance (capacitance on nodes out_p and out_n).

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Analog supply voltage	V_{dd}	-	3.0	3.3	3.6	V
Operating temperature range	T	-	-60	27	100	°C
Differential output voltage	V_{OD}	V_{IOP}- V_{ION} , transmitter mode	300	320	340	mV
Differential output voltage	V_{OD}	V_{IOP}- V_{ION} , transmitter mode, x2i=1	305	320	335	mV
Output offset voltage	V_{OS}	-	1.88	1.2	1.22	V
Line short circuit current	I_{sa},I_{sb}	V_{IOP} and V_{ION} shorted to ground	-	-	3.2	mA
Pair short circuit current	I_{sab}	V_{OUTP} shorted to V_{OUTN}	-	-	3.2	mA
DC power current from V_{dd}	W_{DC}	Transmitter mode, en_rx=0	3.5	3.5	3.5	mA
Total DC power	P_{total}		10.5	11.5	12.6	mW
Rise time	t_{RT}	20% to 80%, transmitter mode, C_{LTX}=1p	132	134	154	ps
Fall time	t_{FT}		131	133	153	ps
Differential time propagation delay, high to low	t_{PHL}	Transmitter mode, C_{LTX}=1p	0.92	1.29	2.1	ns
Differential time propagation delay, low to high	t_{PLH}		0.92	1.29	2.1	ns
Differential skew between t_{PHL} and t_{PLH}	t_{skew1}		-	-	20	ps
AC power current from V_{dd}	I_{VDD}	Transmitter mode, en_rx=0, F_s=600 MHz	5.5	6.0	6.4	mA
Total AC power	W_{AC}		16.5	19.8	23	mW
Clock jitter, rms	t_{RJ}	Transmitter mode, en_rx=0, F_s=600 MHz	256	375	665	fs
Clock jitter, max (p-p)	t_{DJM}		1.6	2.4	4.1	ps
Data jitter, deterministic	t_{DJ}		0.3	1.9	3.2	ps

Table “Electrical characteristics” (continue)

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Data jitter, deterministic crossing ±100mV	t_{DJC}	Transmitter mode, en_rx=0, F_s=600 MHz	60	62.5	72	ps
Input voltage range (common-mode)	V_{in}	Receiving mode	0	-	2.4	V
Input differential threshold	V_{th}		-	-	100	mV
Input impedance	Z_{in}	-	90	100	110	Ohm
DC power current from V_{dd}	W_{DC}	Receiving mode, en_tx=0	1.49	1.64	1.75	mA
Total DC power	P_{total}		4.5	5.4	6.3	mW
Differential time propagation delay, high to low	t_{PHL}	Receiving mode, C_L=50f, V_{ind}=100mV	0.69	0.9	1.6	ns
Differential time propagation delay, low to high	t_{PLH}		0.69	0.9	1.6	ns
Clock signal duty cycle	S	Receiving mode, F_s=620 MHz	46	50	54	%
AC power current from V_{dd}	I_{VDD}	Receiving mode, en_tx=0, F_s=600 MHz	2.1	2.3	2.57	mA
Total AC power	W_{AC}		6.3	7.6	9.3	mW
Clock jitter, rms	t_{RJ}	Receiving mode, C_L=50f, V_{ind}=100mV	0.59	0.85	3.3	ps
Clock jitter, max (p-p)	t_{DJM}		3.6	5.2	19.7	ps
Data jitter, deterministic	t_{DJ}		2	4	80	ps
DC power current from V_{dd}	W_{DC}	en_tx=1, en_rx=1,half-duplex mode	4.9	5.1	5.2	mA
Total DC power	P_{total}		14.7	16.8	18.7	mW
OEN to output enable (V_{OS})[1]	T_{OE}	Transmitter	5	7	10	ns
OEN to output disable (V_{OS})[2]	T_{OD}		1.5	2	2.5	ns
Stand-by current	I_{st}	-	0.9	1	12.5	nA
Input voltage high level	V_{IH}	For digital inputs	$0.7V_{dd}$	-	V_{dd}	V
Input voltage low level	V_{IL}		0	-	$0.3V_{dd}$	V

Note: *$|V_{OD}|=|V_{IOP}-V_{ION}|$
$|V_{OS}|=|V_{IOP}+V_{ION}|/2$
ΔV_{OD}= ($|V_{OD}|$ for V_{IOP} height and V_{ION} low) minus ($|V_{OD}|$ for V_{IOP} low and V_{ION} height)
ΔV_{OS} = (V_{OS} for V_{IOP} height and V_{ION} low) minus (V_{OS} for V_{IOP} low and V_{ION} height)
[1] Output recovery to voltage within the offset voltage range
[2] Output drops out of the output offset voltage range

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation