LVDS IPs library

OVERVIEW

180TSMC_LVDS_10 is a library including:

- Transmitter LVDS driver (TX_LVDS);
- Receiver LVDS driver (RX_LVDS);
- Transceiver LVDS driver (RX_TX_LVDS);
- Reference current/voltage generators (RS_TOP).

RX_TX_LVDS driver has five available operation modes: transmitter, receiver, transmitter half-duplex, receiver half-duplex and shutdown.

The RS_TOP block is intended to output reference currents and voltage for RX_LVDS driver, TX_LVDS driver or TX_RX_LVDS driver.

Composing of LVDS library components allows to design a device with up to 16 pairs of data channels and 2 pairs of synchronization channels.

IP technology: TSMC 0.18µm CMOS technology.

IP status: silicon proven.

Total area: RX_LVDS driver – 0.028mm^2; TX_LVDS driver – 0.047mm^2; RX_TX_LVDS driver – 0.063mm^2; RS_TOP – 0.150 mm^2

Features:

- TIA/EIA-644 LVDS standards without hysteresis
- Data transfer rate: up to 500Mbps (DDR MODE)
- 3.3V IO voltage supply
- 1.8V core voltage supply
- 1.8V CMOS input/output logic control signals
- Embedded 1.8V/3.3V level shifters

Applications:

- Point-to-point data transmission
- Multidrop buses
- Clock distribution
- Backplane receiver
- Backplane data transmission
- Cable data transmission

BLOCK DIAGRAM

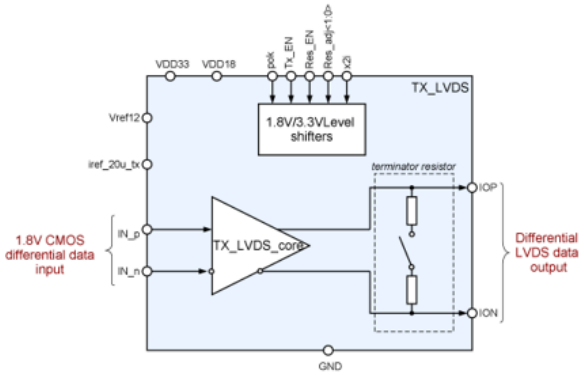

Figure 1: TX_LVDS driver block diagram

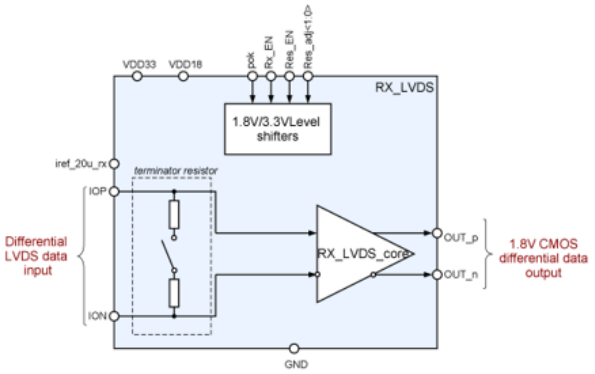

Figure 2: RX_LVDS driver block diagram

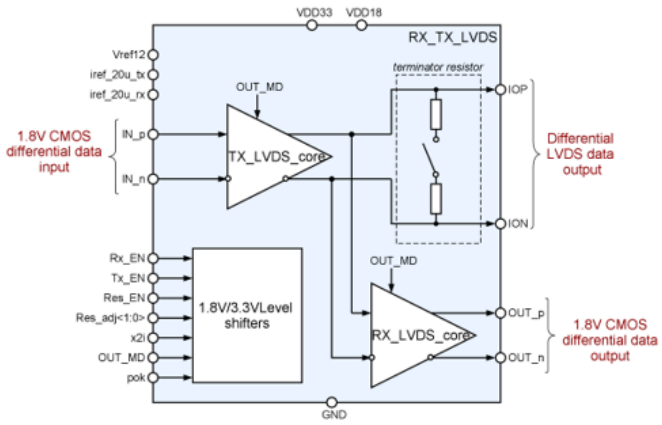

Figure 3: RX TX LVDS driver block diagram

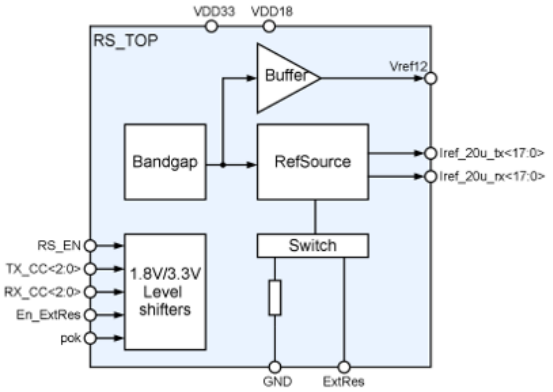

Figure 4: RS TOP block diagram