1 to 100 MHz up-conversion mixer

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- High linearity
- Low power consumption
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- Receivers
- Transmitters

3 OVERVIEW

Device is used to transfer incoming useful intermediate-frequency signal (IF) to high frequencies (RF). Quadrature mixer consists of two double balanced passive mixers, their heterodyne frequencies has 90 degree shift. Scheme in the form of passive mixer provides low supply current and high linearity. Each mixer can be divided into three separated mixers, which phases of heterodyne frequencies have -45, 0, +45 degree shifts, what provides rejection of third and fifth harmonics of high-frequency signal (HR system).

4 STRUCTURE

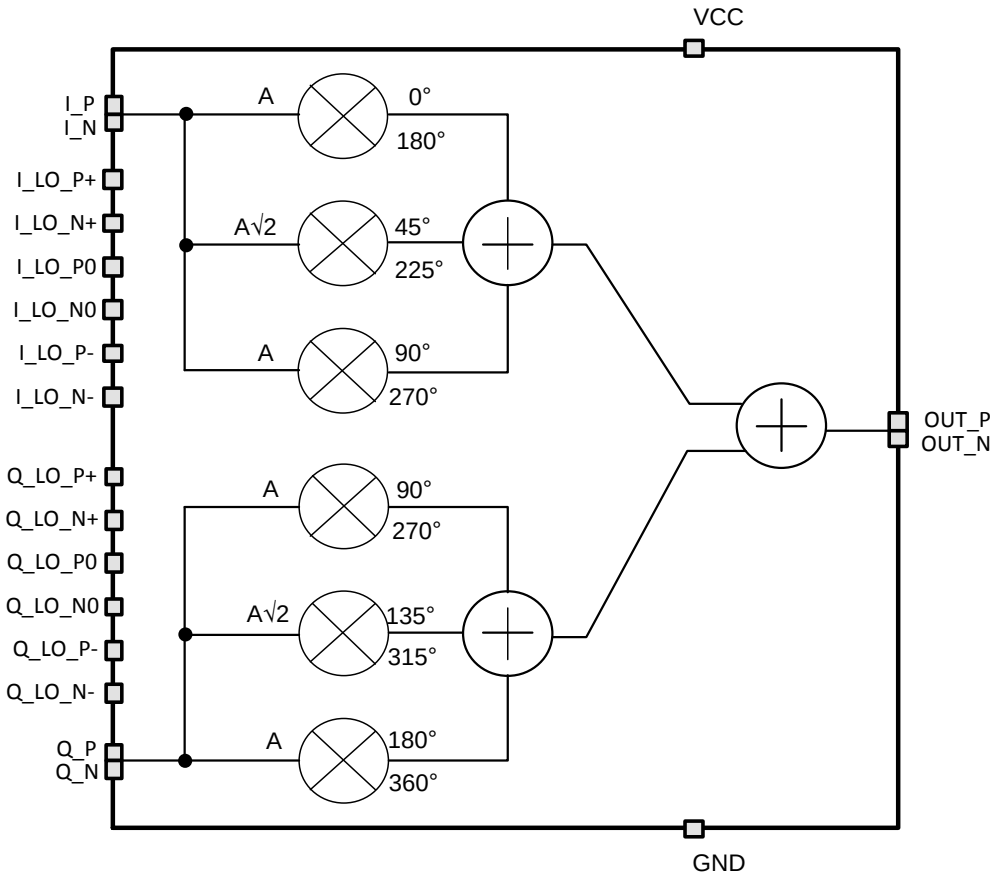

Figure 1: RF passive mixer structure

5 PIN DESCRIPTION

Name	Direction	Description
I_P	I	I channel differential RF mixer input
I_N	I	
Q_P	I	Q channel differential RF mixer input
Q_N	I	
OUT_P	O	Differential RF mixer output
OUT_N	O	
I_LO_P+	I	I channel LO differential input +45°
I_LO_N+	I	
I_LO_P0	I	I channel LO differential input 0°
I_LO_N0	I	
I_LO_P-	I	I channel LO differential input -45°
I_LO_N-	I	
Q_LO_P+	I	Q channel LO differential input +45°
Q_LO_N+	I	
Q_LO_P0	I	Q channel LO differential input 0°
Q_LO_N0	I	
Q_LO_P-	I	Q channel LO differential input -45°
Q_LO_N-	I	
VCC	IO	Supply voltage
GND	IO	Ground

6 LAYOUT DESCRIPTION

Mixer dimensions are given in the table 1.

Table 1: Block dimension

Dimension	Value	Unit
Height	1170	µm
Width	420	µm

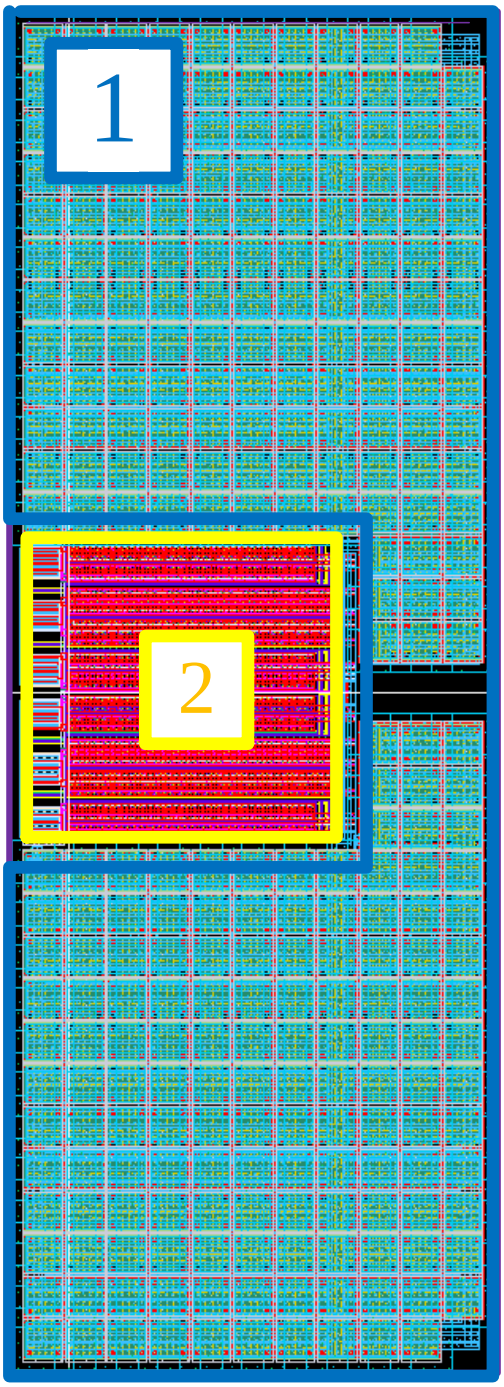

Figure 2: Mixer layout

1. Decoupling capacitors
2. Mixer

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC CMOS CRN65LP
Status _____ silicon proven
Area _____ 0.49 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.14÷ 1.26 V and Ta = -40 ÷ 125 °C. Typical values are at V_{cc} = 1.2 V, Ta = +85 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	1.14	1.2	1.26	V
Operating temperature range	Ta	-	-40	85	125	°C
Input frequency range	F_{IN}	-	-	-	100	MHz
Local-oscillator frequency	F_{osc}	-	100	-	2975	MHz
Output frequency range	F_{OUT}	-	75	-	3000	MHz
Conversion gain	G	F=75 MHz, F_{LO}=10 MHz	-	-9.7	-	dB
		F=1500 MHz, F_{LO}=10 MHz	-	-9.4	-	
		F=3000 MHz, F_{LO}=10 MHz	-	-9.4	-	
Input 1dB compression point	P_{1dB}	F=75 MHz, F_{LO}=10 MHz	-	9.5	-	dBm
		F=1500 MHz, F_{LO}=10 MHz	-	8.9	-	
		F=3000 MHz, F_{LO}=10 MHz	-	8	-	
Linear output third-order intercept point	OIP3	F=75 MHz, F_{LO}=10 MHz	-	24.5	-	dBm
		F=1500 MHz, F_{LO}=10 MHz	-	25.7	-	
		F=3000 MHz, F_{LO}=10 MHz	-	20.5	-	
Input impedance	R_{in}	-	-	25	-	Ohm
Output impedance	R_{out}	-	-	25	-	Ohm
Current consumption in an active mode	I_{cc}	F=75 MHz, F_{LO}=10 MHz	-	0.6	-	uA
		F=1500 MHz, F_{LO}=100 MHz	-	7.1	-	
		F=3000 MHz, F_{LO}=100 MHz	-	19	-	
Current consumption in a standby mode	I_{stb}	-	-	170	-	pA
Input logic-high level	V_{IH}	For digital inputs	0.85V_{cc}	2.5	1.15V_{cc}	V
Input logic-low level	V_{IL}		-0.2	0	+0.2	V

8 TYPICAL CHARACTERISTICS

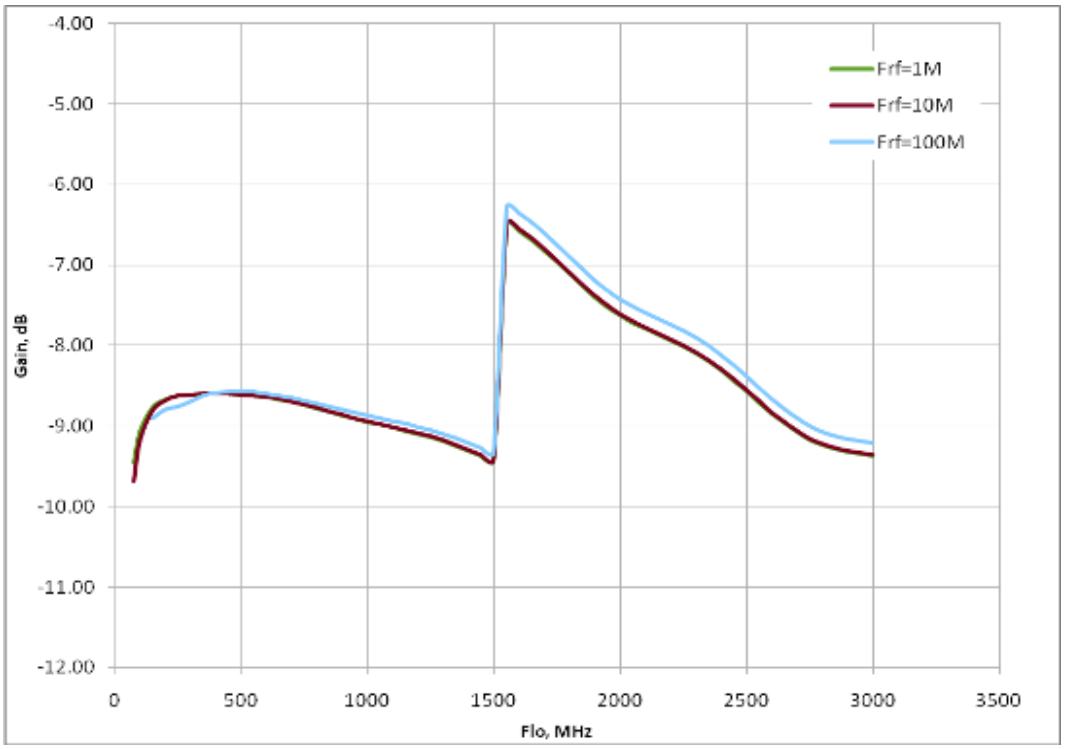

Figure 3: Gain

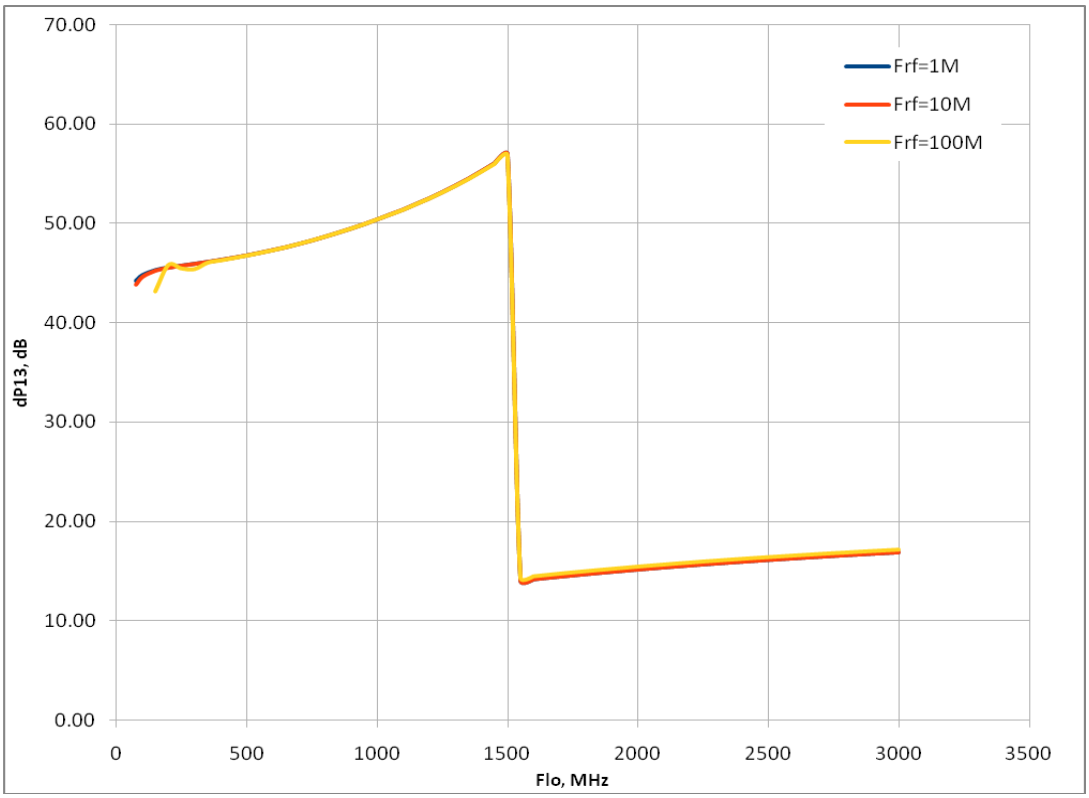

Figure 4: Third harmonic rejection

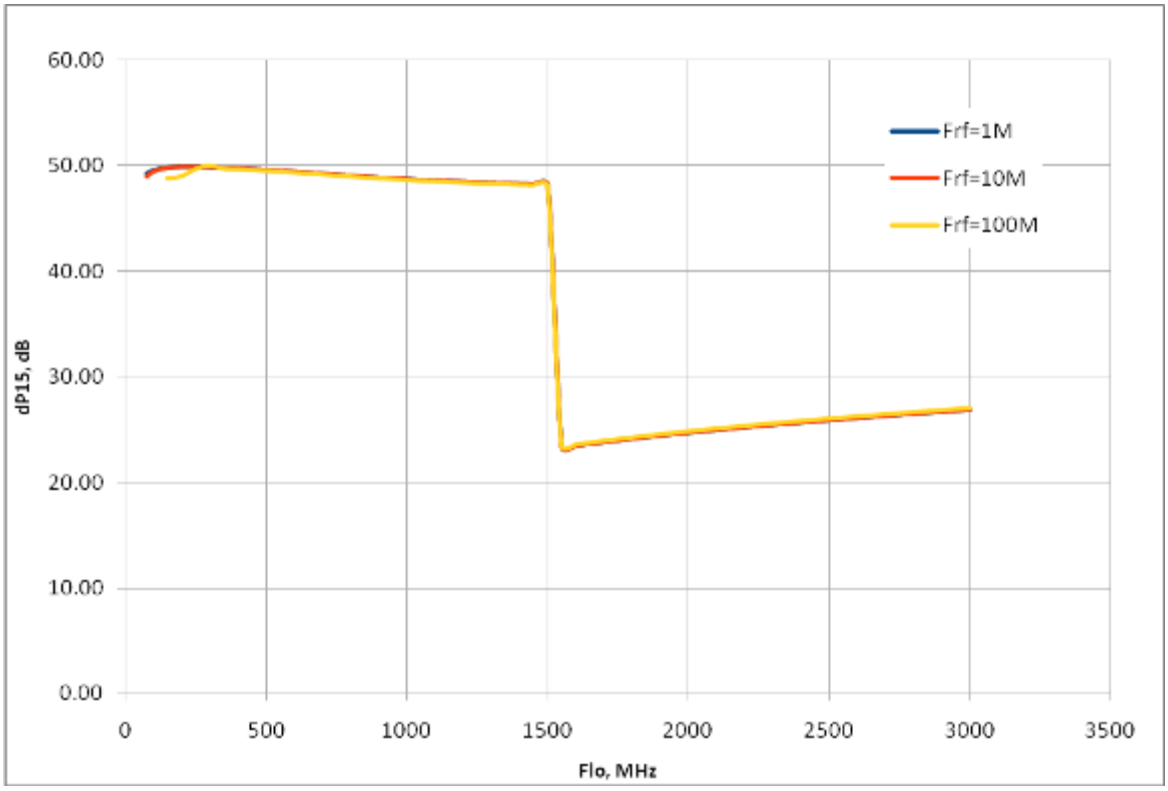

Figure 5: Fifth harmonic rejection

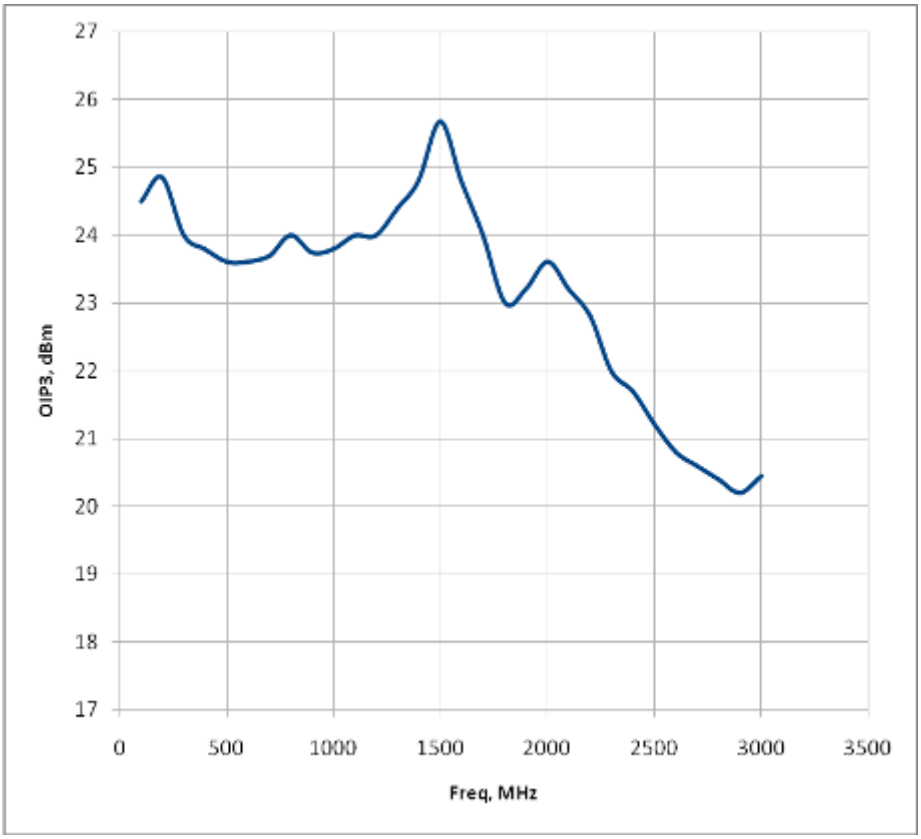

Figure 6: Output third-order intercept point

9 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation