Frequency multiplier

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Wide frequency range from 120 to 950 MHz
- Low current consumption
- Small area
- Operating frequency selection using external components
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

2 APPLICATION

- Frequency synthesizer
- Functional signal generator

3 OVERVIEW

A frequency multiplier is a circuit that generates an output signal whose output frequency is a harmonic of its input frequency. Frequency multipliers consist of a nonlinear circuit that distorts the input signal and consequently generates harmonics of the input signal. An input filter and output resonance circuit select the desired harmonic frequencies and remove the unwanted fundamental and other harmonics from the output.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

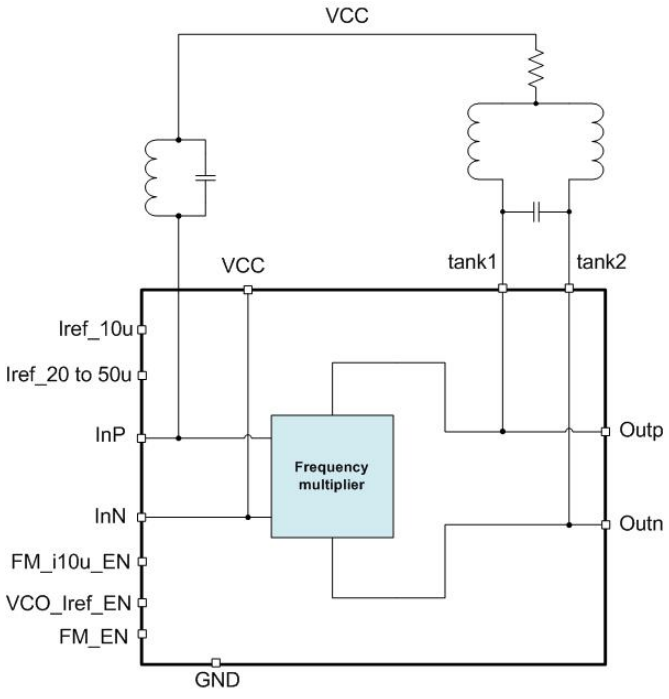

Figure 1: Frequency multiplier structure.

5 PIN DESCRIPTION

Name	Direction	Description
Iref_10u	IO	Reference current (10 uA)
Iref_20to50u	IO	Reference current (20…50 uA)
InP	I	Analog differential input
InN	I	
FM_i10u_EN	I	Frequency multiplier reference current enable
VCO_Iref_EN	I	Reference current enable
tank1	IO	LC tank
tank2	IO	
Outp	IO	Analog differential output
Outn	IO	
GND	IO	Ground
VCC	IO	Supply voltage

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions.

Name	Direction	Description
Height	189	um
Width	304	um

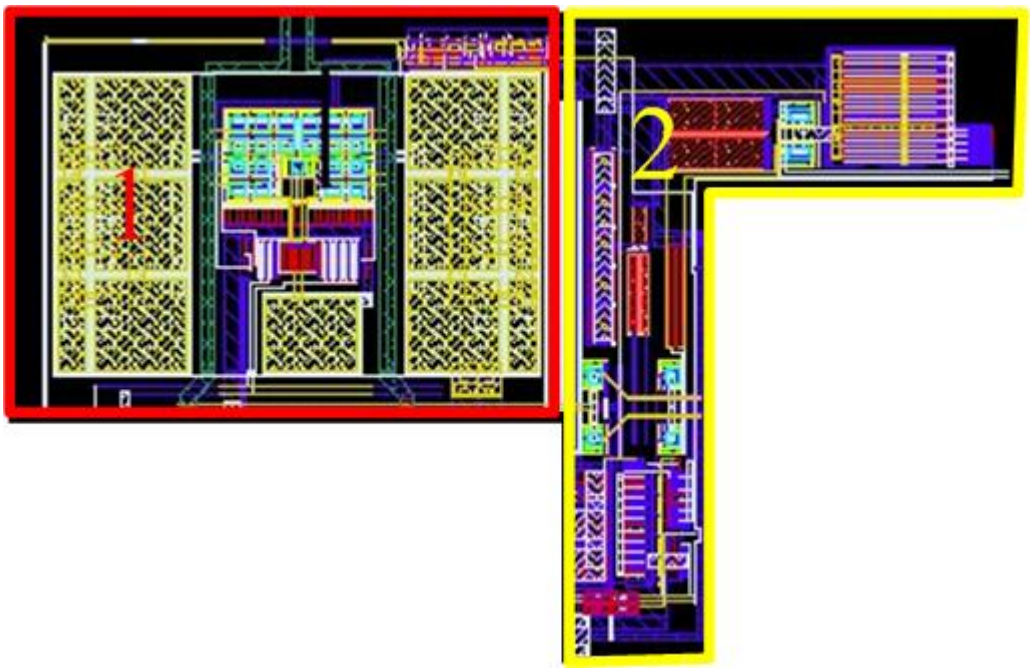

Figure 2: Device layout view.

1. Frequency multiplier
2. Frequency multiplier output buffer

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.25 um
Status _____ silicon proven
Area _____ 0.027 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.9 ÷ 2.3 V and T_a = -45 ÷ +85 °C. Typical values are at V_{cc} = 2.2 V and T_a = +27° C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	1.9	2.2	2.3	V
Operating temperature range	T_a	-	-45	27	85	°C
Output frequency*	F_{FM}	-	120	-	950	MHz
Output amplitude	A_{FM}	-	300	-	-	mV
Peak-to-peak differential input voltage	$A_{in\ p\text{-}p}$	-	350	550	-	mV
Input DC operating point	U_{in}	-	-	1.5	-	V
Output DC operating point	U_{out}	-	-	1.5	-	V
Current consumption in an active mode	I_{cc}	173MHz	-	495	-	uA
		470MHz	-	880	-	
Current consumption in a standby mode	I_{stb}	-	-	1	10	nA
Input logic-high level	V_{IH}	For digital inputs	$0.7V_{cc}$	-	V_{cc}+0.25	V
Input logic-low level	V_{IL}		-0.25	-	0.3	V

*Output frequency value is defined by an input frequency and external component values.

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation