

## Multiplexer - amplifier

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### SPECIFICATION

#### 1 FEATURES

- SMIC CMOS 0.18 $\mu$ m
- Differential output
- Mode of signal injection at one of the output
- Input and output matching 50  $\Omega$
- No external matching components required
- Manual adjustment of matching
- Gain temperature compensation mode
- Portable to other technologies (upon request)

#### 2 APPLICATION

- Multiplex navigation receiver

#### 3 OVERVIEW

The cell is combined into one block multiplexer, amplifier and splitter. The multiplexer selects one of the required inputs by a combination of control signals. Splitter transmits the amplified signal to either one or both outputs.

Temperature compensation mode is used to compensate gain vs. environment temperature. The block is fabricated on SMIC CMOS 0.18 $\mu$ m technology.

## 4 STRUCTURE

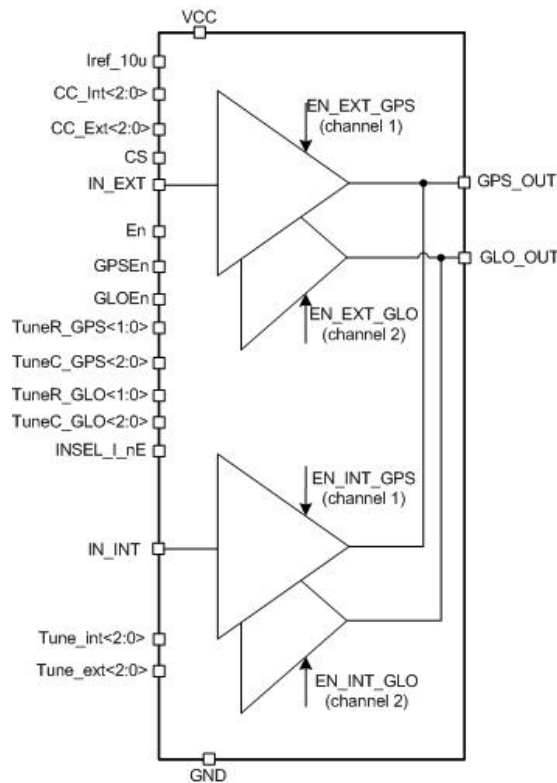


Figure 1: Multiplexer - amplifier structure.

## 5 PIN DESCRIPTION

Name	Direction	Description
Iref_10u	I	Reference current (10 $\mu$ A)
CC_Int<2:0>	I	Amplifier current control in an active antenna mode
CC_Ext<2:0>	I	Amplifier current control in an external low-noise amplifier mode
CS	I	Temperature compensation mode enable
En	I	Enable/disable
GPSEn	I	1 <sup>st</sup> channel enable/disable
GLOEn	I	2 <sup>nd</sup> channel enable/disable
TuneR_GPS<1:0>	I	1 <sup>st</sup> channel output circuit impedance adjustment
TuneC_GPS<2:0>	I	1 <sup>st</sup> channel output circuit capacitor adjustment
TuneR_GLO<1:0>	I	2 <sup>nd</sup> channel output circuit impedance adjustment
TuneC_GLO<2:0>	I	2 <sup>nd</sup> channel output circuit capacitor adjustment
INSEL_I_nE	I	Input select
Tune_int<2:0>	I	External active antenna input adjustment
Tune_ext<2:0>	I	External low-noise amplifier input adjustment
IN_INT	I	External active antenna input
IN_EXT	I	External low-noise amplifier input
OUT_GLO	O	1 <sup>st</sup> channel output
OUT_GPS	O	2 <sup>nd</sup> channel output
VCC	IO	Supply voltage

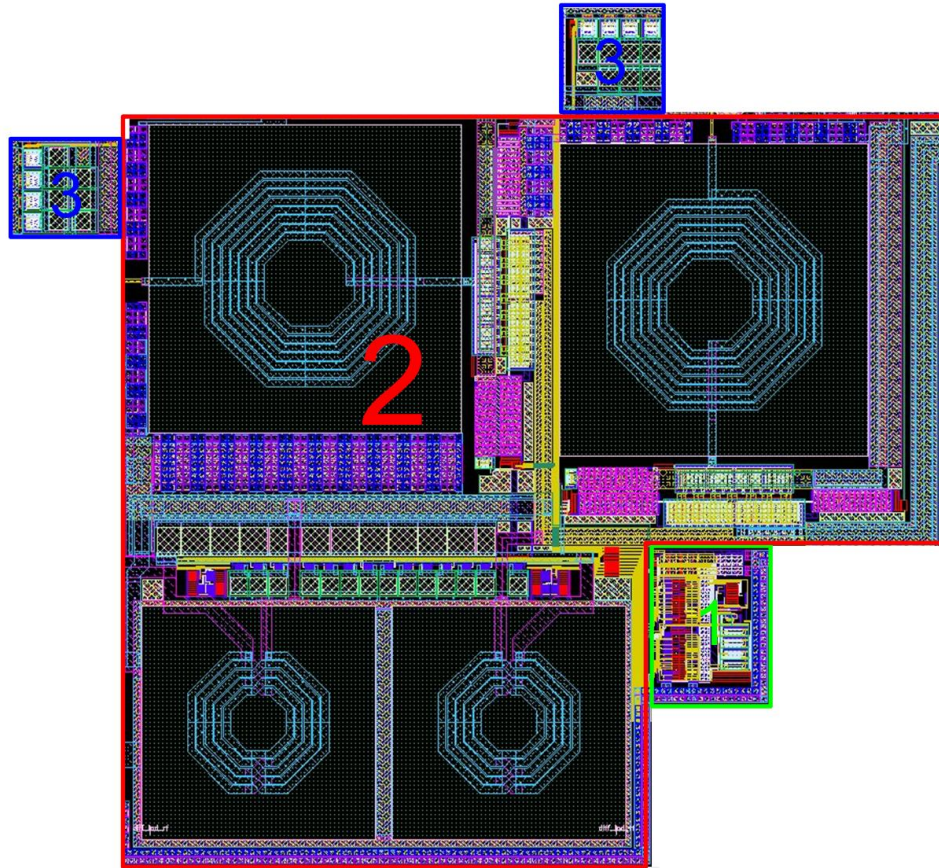
Name	Direction	Description
GND	IO	Ground

## 6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

**Table 1:** Block dimensions.

Dimension	Value	Unit
Height	937.2	$\mu\text{m}$
Width	1030.92	$\mu\text{m}$



**Figure 2:** Device layout view.

1. Reference current source
2. Amplifying splitter
3. Tuned capacitors

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ SMIC CMOS 0.18  $\mu\text{m}$   
 Status \_\_\_\_\_ silicon proven  
 Area \_\_\_\_\_  $0.7\text{mm}^2$

### 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{cc} = 1.7 \div 1.9\text{ V}$  and  $T = -45 \div +85\text{ }^\circ\text{C}$ . Typical values are at  $V_{cc} = 1.8\text{ V}$  and  $T = +27\text{ }^\circ\text{C}$ , unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	$V_{cc}$	-	1.7	1.8	1.9	V
Operating temperature range	T	-	-45	27	85	$^\circ\text{C}$
Input frequency range	$F_{in}$	Band L1	1571	-	1579	MHz
		Band L2	1598	-	1606	
Input VSWR	$VSWR_{MA\_IN}$	-	-	1.1	2.0	-
Output VSWR	$VSWR_{MA\_OUT}$	-	-	1.6	2.0	-
Input 1dB compression point *	$P_{1dB\_MA}$	-	-	-10	-	dBm
Insertion loss	$G_{MA}$	-	-	7	-	dB
Noise figure	$NF_{MA}$	-	-	4.5	-	dB
Current consumption in an active mode	$I_{cc}$	With one output	-	2.7	-	mA
		With 2 outputs	-	5.1	-	
Current consumption in a standby mode	$I_{stb}$	-	-	3	860	nA
Input logic-high level	$V_{IH}$	For digital inputs	$0.7 V_{cc}$	-	3.6	V
Input logic-low level	$V_{IL}$		-0.25	-	0.3	V

\* For inputs IN\_INT and IN\_EXT

## 8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

## REVISION HISTORY

1. From version 1.0:
  - Table “Electrical characteristics” (refer to [page 4](#))
  - Added parameter “Input frequency range”