Power on reset with detector

SPECIFICATION

1 FEATURES

- Global Foundries CMOS 55 nm
- Low current consumption
- Small area
- Can be ported to foundries TSMC, UMC, SMIC, iHP, AMS, Vanguard, SilTerra and other also compatible to with different technology nodes[1]

2 APPLICATIONS

- Power on reset
- Supply voltage level detector

3 OVERVIEW

Power on reset with detector produces a reset signal at power up. The block consists of voltage detector, power on reset and digital cell NOR3. The voltage detector is a comparator that compares input voltage with reference voltage. The power on reset is a special circuit that generates a signal after rising supply voltage required for the initial state of the triggers.
The block is designed on Global Foundries CMOS 55 nm technology.

[1] For more information contact NTLab

4 FUNCTIONAL DESCRIPTION

If the block is used standalone, you need connect signal bg_startn to pin vcc. For best results, the block must be used together with IP 055GF_BVR_01, using its output signals: startn, vref and any from iref1 to iref10. Output signal with power on reset appears after rising supply voltage. Output signal with voltage detector appears by comparing voltage 1.3 V. Signal bg_startn, output signal with power on reset and output signal with voltage detector are fed to inputs of digital cell NOR3. Low level signal at the output of digital cell NOR3 corresponds to reset, high level signal at the output of digital cell NOR3 corresponds to the normal operation.

4.1 PIN FOR OUTPUT SIGNAL

Pin for output signal is Power on reset with detector output pin out. Output pin out assumes a capacitive load up to 1 pF. By increasing the load capacitance will increase delay of output signal.

5 STRUCTURE

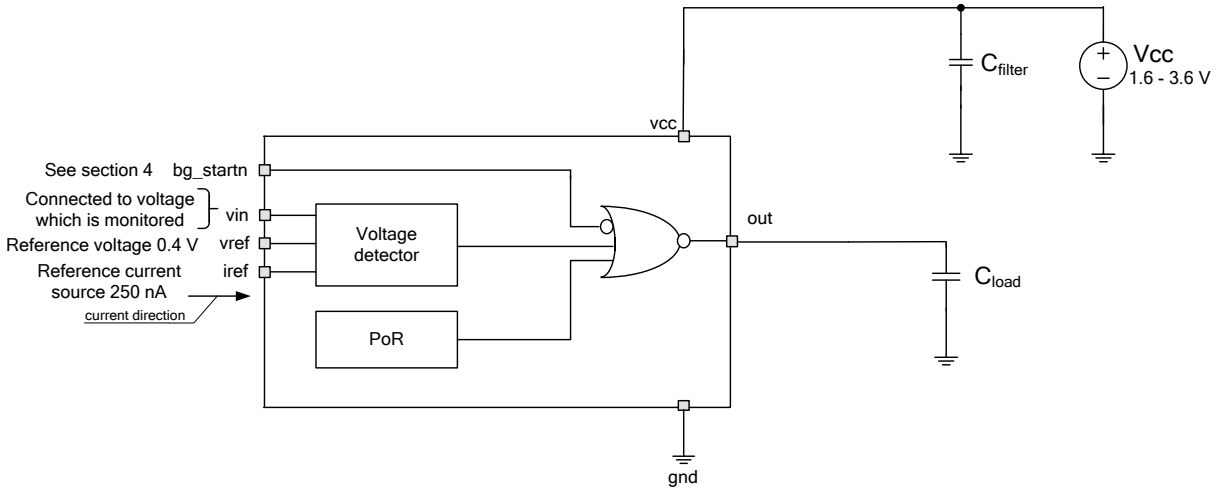

Figure 1: Power on reset with detector structure and application diagram

6 PIN DESCRIPTION

Name	Direction	Description
iref	IO	Reference current 250 nA
bg_startn	I	Input for hold output
vin	I	Detector input
vref	I	Reference voltage 0.4 V
out	O	Output PoR
vcc	IO	Supply voltage
gnd	IO	Ground

Note: * I – input, O – output

7 LAYOUT DESCRIPTION

7.1 TECHNOLOGY OPTIONS

Power on reset with detector is designed under Global Foundries CMOS 55 nm technology process with following options:

- 4_02_00_00_LB option
- 2 metal levels of 1x (thin) width are used for routing
- Thick-oxide I/O NFET and PFET (3.3 V)
- P+ polysilicon OP resistor

7.2 PHYSICAL DIMENTIONS

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	50.8	um
Width	88.3	um

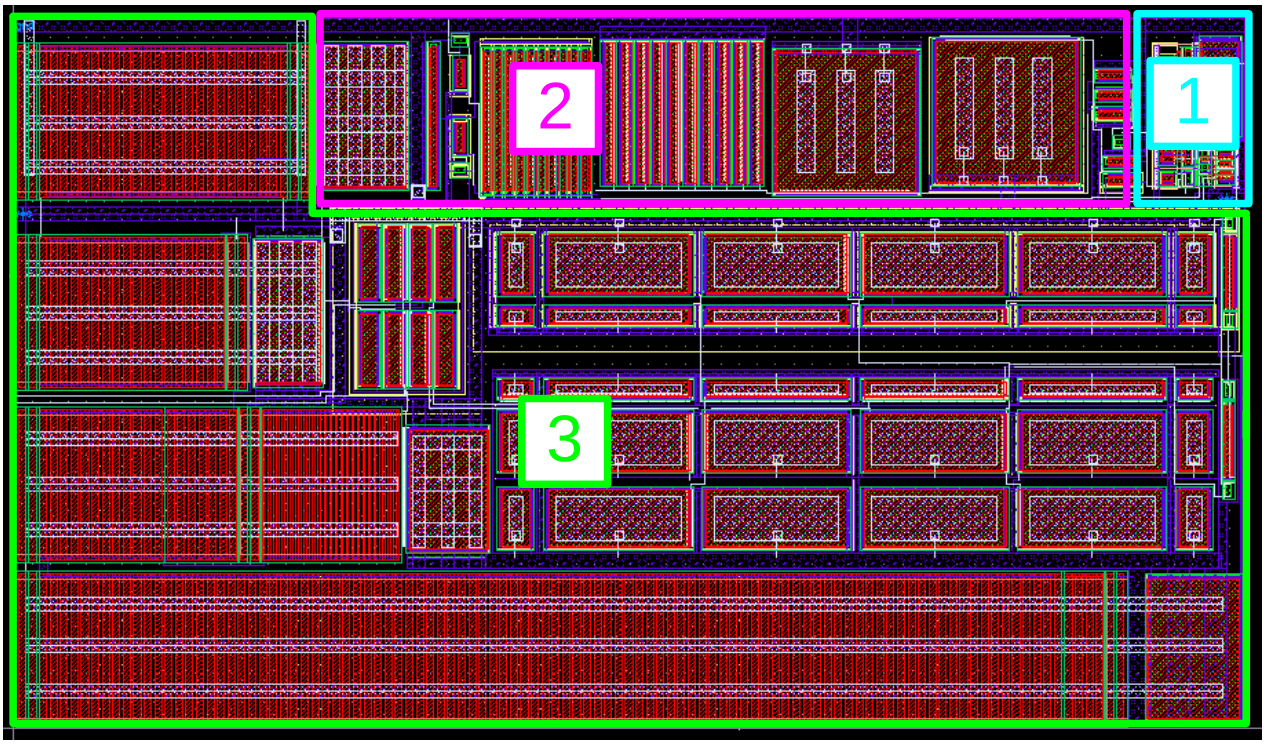

Figure 2: Power on reset with detector layout

1. NOR3 gate
2. Power on Reset
3. Voltage detector

8 INTEGRATION GUIDELINES

8.1 INPUT AND OUTPUT SIGNALS

Capacitance of pin bg_startn is 10 fF.
Capacitance of pin out is 20 fF.

8.2 PLACEMENT AND ROUTING

The following recommendations are given:

1. Power on reset with detector layout can be rotated and flipped in axis X and Y
2. Power supply (pin vcc) and ground (pin gnd) wires should allow flowing of 0.1 mA DC, 0.5 mA peak currents and should have resistance of less than 10 Ohm between pins and pads
3. For best results, use capacitance connected between power supply and ground
4. Wire for input pin vin must be connected to a block supply voltage for monitoring and must be shorter to avoid changes in the threshold detector
5. Is necessary to avoid parasitic capacitance coupling to the wire between reference current source and pin iref and wires, which have digital signals, as this can lead to a stable output pulsations voltage. If there is a need to conduct the connecting wires over the wire between reference current source and pin iref, it is necessary to apply the metal shielding of the wire. Shielding metal should be connected to the ground
6. No routing is allowed over the block in layers M1—M2

Other pins, not described here, have no special routing guidelines.

8.3 LAYOUT VERIFICATION

- DRC and LVS are run using Mentor Graphics Calibre
- No dummy structures are required for layers PC, RX, M1—M2

9 OPERATION CHARACTERISTICS

9.1 TECHNICAL CHARACTERISTICS

Technology Global Foundries CMOS 55 nm
Status silicon proven
Area 0.0045 mm^2

9.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.6 ÷ 3.6 V, Vref = 400 mV, Iref = 250 nA and T_j = -40 ÷ +85 °C. Typical values are at V_{cc} = 2.5 V and T_j = 27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	1.6	2.5	3.6	V
Operating temperature range	T_j	-	-40	27	+85	°C
Detect threshold	V_{TH}	-	1.235	1.3	1.365	V
Current consumption	I_{cc}	-	-	-	2	uA
Input logic-level low	V_{IL}	For digital signals	0	-	$0.3*V_{cc}$	V
Input logic-level high	V_{IH}		$0.7*V_{cc}$	-	V_{cc}	
Output logic-level low	V_{OL}		0	-	$0.2*V_{cc}$	
Output logic-level high	V_{OH}		$0.8*V_{cc}$	-	V_{cc}	

10 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

11 REVISION HISTORY

From version 1.0:

- Section 3 “Overview” updated
- Section 4 “Structure” shifted to section 5
- Section 4 “Functional description” added
- Section 5 “Structure”. Figure 1 updated
- Subsection 7.1 “Technology options” updated
- Subsection 7.2 “Physical dimensions” updated
- Section 8 “Integration guidelines” updated
- Section 9 “Operation characteristics” updated
- Subsection 9.2 “Electrical characteristics”:
  - Parameters “Input logic-level high” and “Input logic-level low” were added
- Section 10 “Deliverables” updated