Power on Reset

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- Input voltage range: from 1.1 V to 1.3 V
- Embedded Bandgap with Reference current source
- Low quiescent current
- Supported foundries: TSMC, UMC, Global Foundries

2 APPLICATION

- Core voltage low battery indication
- Supply voltage sensitive circuits
- Battery-Powered equipment
- Power solutions

3 OVERVIEW

Power-on-Reset (PoR) circuit provides a reset signal to the chip when supply voltage reach required level. PoR generates reset signal depending of the level supply voltage with hysteresis. It includes Bandgap with Reference current and Power on Reset block

4 STRUCTURE

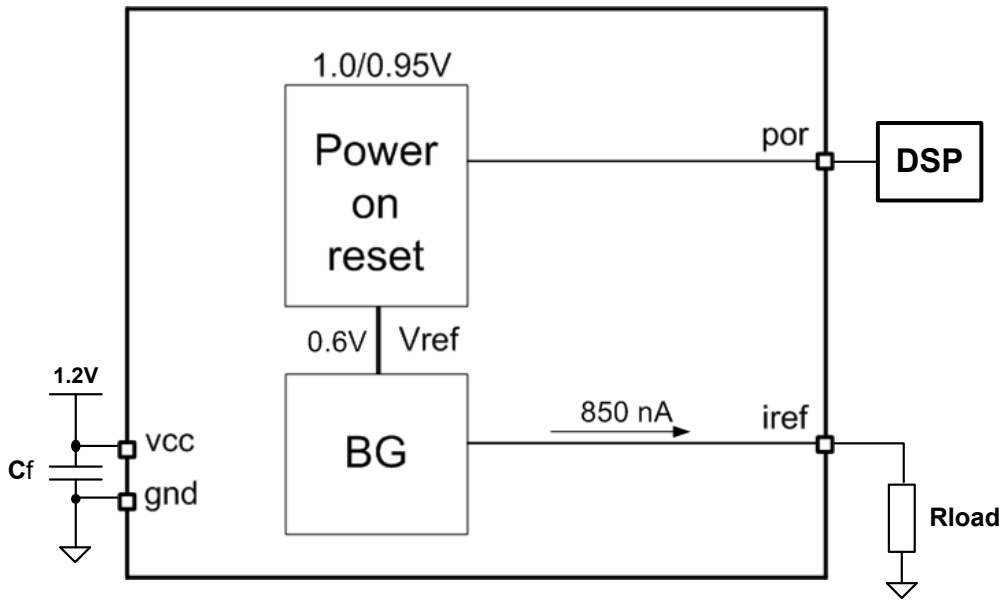

Figure 1: PoR structure with application schematic

4.1 POR FUNCTION DIAGRAMM

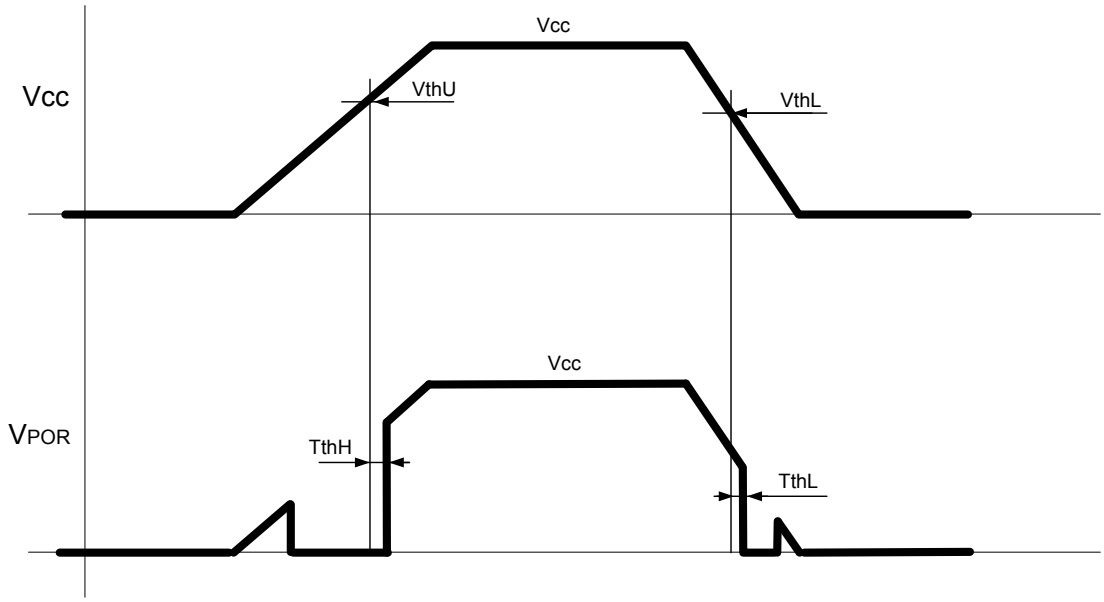

Figure 2: PoR output signal

5 PINS DESCRIPTION

Name	Direction	Description
iref	O	Reference current 850 nA
por	O	Power on reset logical output signal
vcc	P	Power supply 1.2V
gnd	P	Ground

6 LAYOUT DESCRIPTION

6.1 TECHNOLOGY OPTIONS

PoR is designed under TSMC 65nm LP (CLN65LP) technology process with following options and elements:
- 4 metal levels are used for routing
- 2.5V native NMOS transistors
- 2.5V nominal VT PMOS and NMOS transistors
- Vertical PNP bipolar transistor
- P+ poly resistor without salicide

6.2 PHYSICAL DIMENSIONS

The block dimensions are given in the table

Dimension	Value	Unit
Height	146	um
Width	425	um

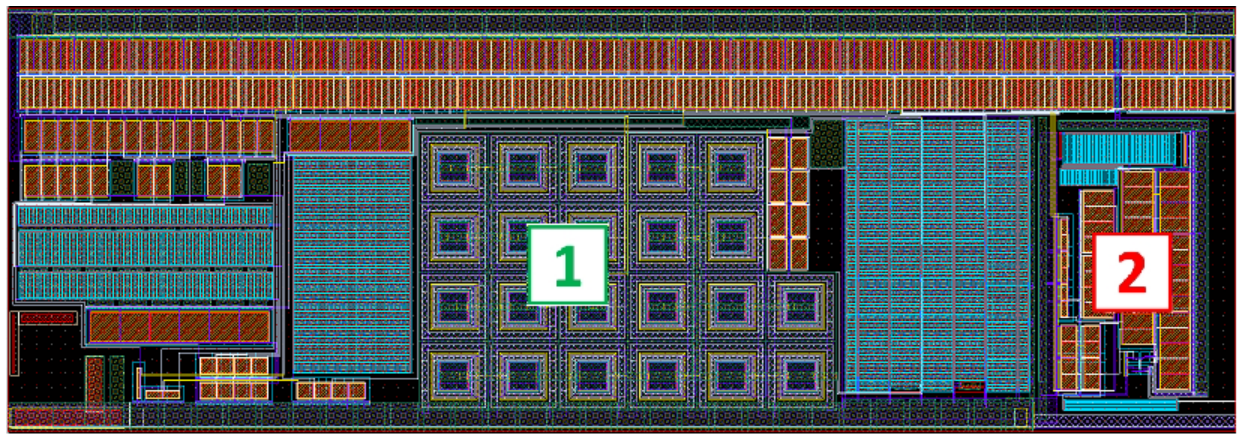

Figure 3: PoR layout structure

1. Bandgap with Reference current source
2. Power on reset

7 INTEGRATION GUIDELINES

7.1 INPUT AND OUTPUT SIGNALS

Output signals have intrinsic capacitance up to 20 fF.
Output signals rising/falling edges depends on additional capacitance connected to these pin at integration level. The formula of slopes is

$$Time = Kload*(Crouting+20fF),$$

where 20 fF comes from intrinsic capacitance, *Crouting* is routing capacitance and *Kload* is as follows:

	Kload, ns/pF	
	rise	**fall**
Typical value	1.25	0.91

7.2 PLACEMENT AND ROUTING

PoR is an analog block, which is sensitive to power supply, ground and substrate noise. So, the following recommendations are given.

1. PoR layout can be rotated and flipped in axis X and Y
2. IP should be used in the 1.2 voltage domain
3. Power supply (pin vcc) and ground (pin gnd) wires should allow flowing of 0.5 mA DC, 1 mA peak currents and should have resistance of less than 2 Ohm
4. External capacitance 0.25—0.5nF and internal capacitance should be connected to Vcc pin for additional noise filtering. Internal capacitance should be added as much as possible
5. Pitch between PoR and Iref output path and any clocking or noisy signals paths should be more than 7 um
6. No routing is allowed over the block in layers M1—M4

7.3 LAYOUT VERIFICATION

- DRC and LVS are run using Mentor Graphics Calibre
- No dummy structures are required for layers PO, OD, M1—M4

8 OPERATING CHARACTERISTICS

8.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS 65 nm
Status silicon proven
Area 0.062 mm^2

8.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for Vcc = 1.1 ÷ 1.3 V and Tj = -40 ÷ +85°C. Typical values are at Vcc = 1.2V, Tj = +27°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Voltage supply	V_{CC}	-	1.1	1.2	1.3	V
Operating temperature range	Tj	-	-40	+27	+85	°C
Threshold Power on reset voltage	V_{THU}	See fig. 2	-	1.001	-	V
	V_{THL}		-	0.952	-	
Reference current	I_{ref}	-	720	845	1003	nA
Time delay	$T_{TH}H$	See fig. 2	-	0.4	-	ns
	$T_{TH}L$		-	1.2	-	ns
Current consumption	I_{CC}	Vcc = 1.2 V	9	11	14	uA
Current consumption in standby mode	I_{stb}	-	-	35	-	pA
Output logic-level high	V_{OH}	-	0.8 V_{cc}	-	1.3	V
Output logic-level low	V_{OL}	-	-0.1	-	0.3	

9 DELIVERABLES

Depending on license, type IP may include:

- Schematic or NetList
- Layout or blackbox
- Verilog, lef and lib files
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.3:

- Section 3 updated
- Section 4 updated:
  - PoR structure with application schematic was updated
- Subsection 4.1 updated:
  - Added figure 2: PoR output signal
- Subsection 6.1 updated
  - Number routing metal changed from 7 to 4
  - Added figure 2: PoR output signal
- Subsection 7.2 updated:
  - Added placement rules
- Subsection 7.3 updated:
  - Update verification rules
- Subsection 7.5 updated:
  - Time delay parameter added
  - Min voltage supply from 0.9 to 1.1V was changed
  - Parameter name Power on reset voltage to Threshold Power on reset voltage changed
  - Output logic-level high and low value updated
- Section 8 updated

From version 1.2:

- Section 6.2 updated:
  - Changed physical block dimension
- Subsection 7.1 integration guidelines

From version 1.1:

- Subsection 4.1 added
- Subsection 6.1 added