Power on Reset

SPECIFICATION

1 FEATURES

- TSMC018 SiGe BiCMOS 0.18 µm
- Low current consumption
- Small layout area
- Portable to other technologies (upon request)

2 APPLICATION

- Power on reset

3 OVERVIEW

The power on reset consists of a Schmitt trigger and simple logic for forced reset input, whish is forced asynchronous reset. Output port is $\overline{\text{Reset}}$, that means it is low to set flip-flop in particular state.
The block is fabricated in TSMC018 SiGe BiCMOS 0.18 µm.

4 STRUCTURE

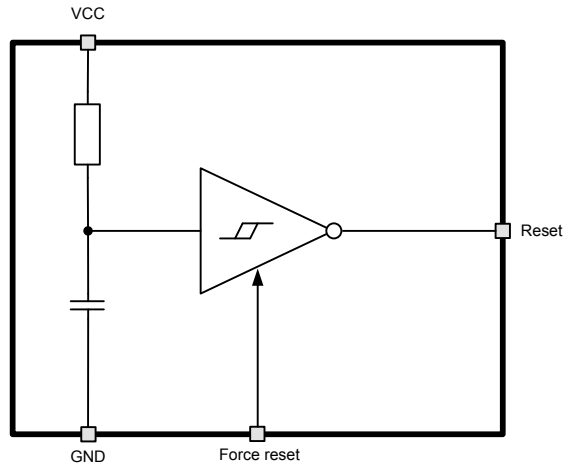

Figure 1: Power on Reset structure.

5 PIN DESCRIPTION

Name	Direction	Description
ResetPad	I	Forced asynchronous reset. Active high.
ResetN	O	Output reset. Active - low, high level in normal mode.
VCC	IO	Supply voltage
GND	IO	Ground

6 LAYOUT DESCRIPTION

Power on Reset dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	80	µm
Width	110	µm

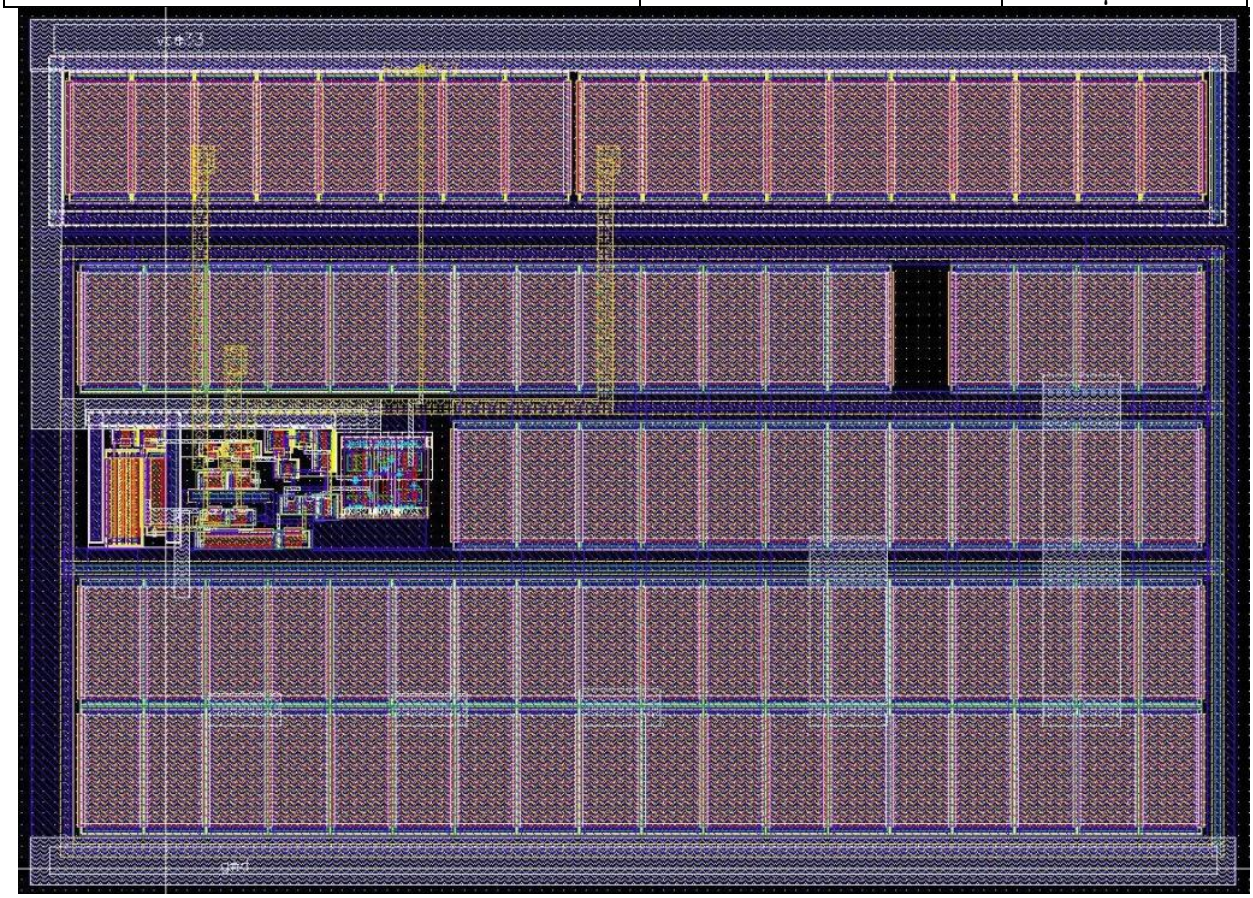

Figure 2: Power on Reset layout view.

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC018 SiGe BiCMOS
Status _____ silicon proven
Area _____ 0.01 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for Vcc = 3.0 ÷ 3.6 V и T = -40 ÷ +85°C. Typical values are at V_{CC} = 3.3 V, T = +27°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	3.0	3.3	3.6	V
Operating temperature range	T	-	-40	+27	+85	°C
Reset threshold voltage	V_{TH}	-	2.5	2.52	2.74	V
Vcc to reset delay	t_{pd}	-	26	50	89	µs
Reset output voltage low	V_{OL}				0.46	V
Vcc suply current	I_{CC}	-	-	-	0.5	nA
Input logic-level high	V_{IH}	Digital inputs	$0.9V_{cc}$	-	$1.1V_{cc}$	V
Input logic-level low	V_{IL}		-0.2	-	0.2	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation