Power amplifier

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- E class PA
- Adjusted gain (-20..10 dBm)
- Built-in voltage regulator
- Built-in duty cycle adjustment system of output signal
- Built-in block of adjustment capacities for fine adjustment characteristics
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

2 APPLICATION

- Portable transmitters
- Portable transceiver
- Mobile communication devices

3 OVERVIEW

The power amplifier transmission of RF signal to the antenna. It is based on E class power amplifier with preamplifier. Voltage regulator and duty cycle adjustment system are used to regulate an output power. Matching circuit is needed to transmit output signal to the antenna and to eliminate the second and the third harmonics of PA output signal. Built-in trimming capacitors are used for PA fine adjustment.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

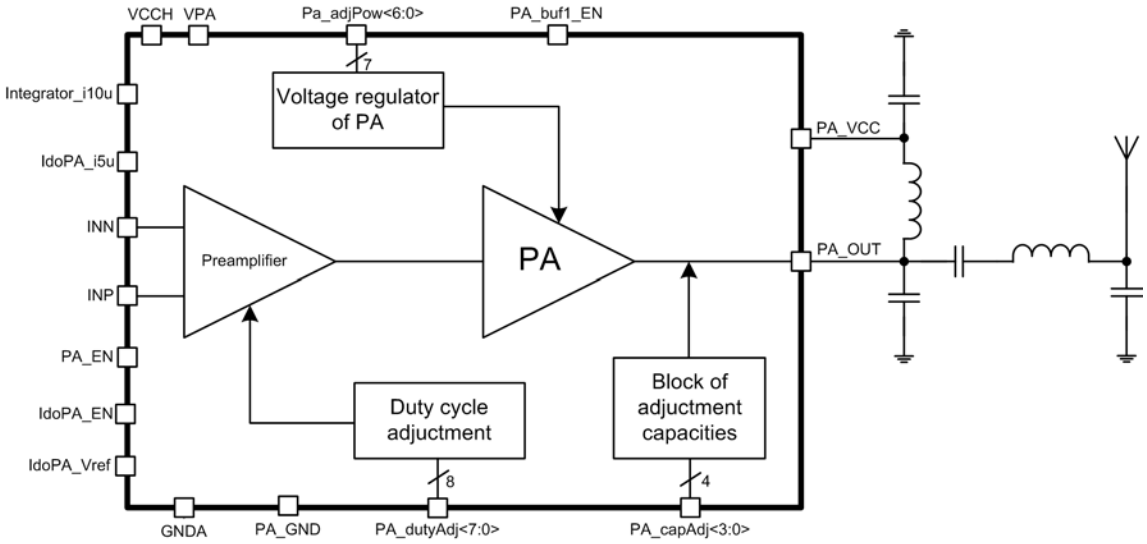

Figure 1: Power amplifier structure.

5 PIN DESCRIPTION

Name	Direction	Description
integrator_i10u	IO	Integrator reference current (10uA)
ldoPA_i5u	IO	Voltage regulator reference current
INN	IO	Analog differential input
INP		
PA_EN	I	PA enable/disable
ldoPA_EN	IO	Voltage regulator enable / disable
ldoPA_Vref	IO	Voltage regulator reference voltage
PA_OUT	IO	PA output
PA_adjPow<6:0>	I	Supply voltage adjustment of PA output transistor
PA_buf1_EN	O	PA buffer enable/disable
Pa_dutyAdj<7:0>	I	Preamplifier output duty cycle adjustment
PA_capAdj<3:0>	I	Output capacity adjustment
PA_VCC	IO	PA supply voltage
VCCH	IO	External supply voltage (1.9 …3.6 V)
VPA	IO	Stabilized supply voltage (1.9 …. 2.3 V)
PA_GND	IO	PA ground
GNDA	IO	Ground

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	713	um
Width	2033	um

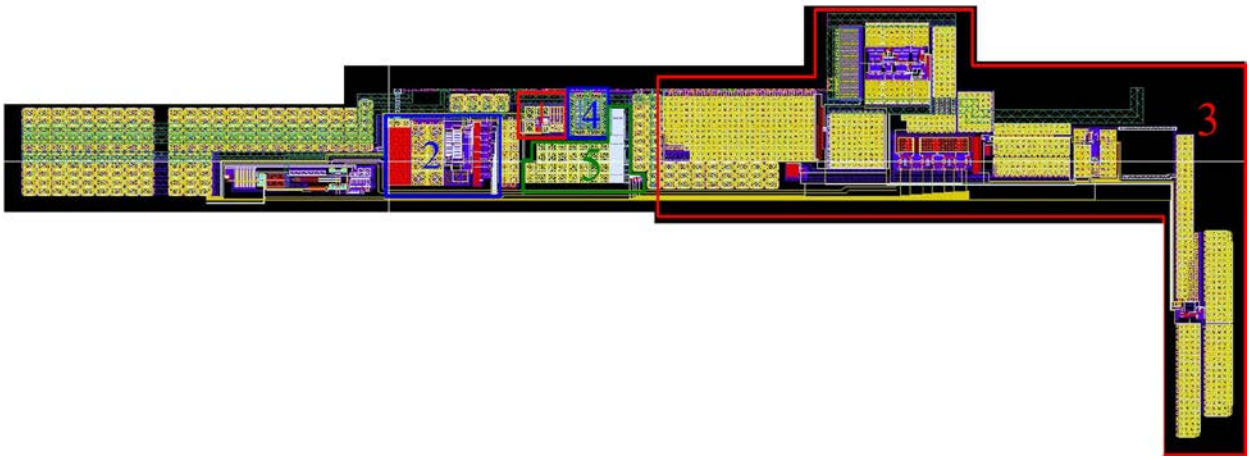

Figure 1: Device layout view.

1. Preamplifier
2. Duty cycle adjustment system
3. PA voltage regulator
4. PA core
5. Trimmer capacitors

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.25 um
Status _____ silicon proven
Area _____ 0.4 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.9 ÷+2.3 V and T_a = -45 ÷ +85 °C. Typical values are at V_{cc} = 2.2 V, T_a = 27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	1.9	2.2	2.3	V
External supply voltage	V_{cch}	-	1.9	2.5	3.6	V
Operating temperature range	T_a	-	-45	27	85	°C
Operating frequency range	F	-	130	-	930	MHz
Output resistance	R_{out}	without matching circuit	-	50	-	Ω
Peak-to-peak differential input voltage	$A_{in\ p\text{-}p}$	-	400	-	1300	mV
DC operating point	U	-	-	400	-	mV
Maximum output power	P_{out_max}	F =130-150 MHz	-	10	-	dBm
		F =300-450 MHz	-	10	-	
		F =905-935 MHz	-	8	-	
Minimum output power	P_{out_min}	F =130-150 MHz	-	-20	-	dBm
		F =300-450 MHz	-	-20	-	
		F =905-935 MHz	-	-20	-	
Relative harmonic level	P_{harm}	F =130-150 MHz	-	-39	-	dB
		F =300-450 MHz	-	-39	-	
		F =905-935 MHz	-	-43	-	
Current consumption in an active mode at maximum power output	I_{ccmaxP}	F =130-150 MHz	-	42.3	-	mA
		F =300-450 MHz	-	38	-	
		F =905-935 MHz	-	23	-	
Current consumption in a standby mode at minimum power output	I_{ccminP}	F =130-150 MHz	-	2.5	-	mA
		F =300-450 MHz	-	5.1	-	
		F =905-935 MHz	-	9	-	
Input logic-high level	V_{IH}	For digital inputs	$0.7V_{cc}$	-	V_{cc}+0.25	V
Input logic-low level	V_{IL}		-0.25	-	0.3	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation