

# Phase frequency detector and charge pump

## SPECIFICATION

### 1 FEATURES

- TSMC018 SiGe BiCMOS
- Input signals with low amplitude
- Low disbalance of output current
- High accuracy
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SiTerra

### 2 APPLICATION

- Phase-locked loop synthesizer

### 3 FUNCTIONAL DESCRIPTION

Phase-frequency detector (PFD) forms a control signal for VCO tuning. PFD compares phases of a divided VCO signal and a divided reference oscillator signal and detects phase difference. Charge pump (CP) generates pulses for the loop filter. The structure consists of two types of PFD with CP: ECL and CMOS choosing by a bit PFD\_TP.

The lock detector monitors the current status of PLL by comparing the phase difference of VCO divided signal and reference oscillator signal with required value. LD\_MP<1:0> and LD\_ACR outputs set the lock monitoring period and the lock detector accuracy, respectively. The block is fabricated on TSMC018 SiGe BiCMOS technology.

### 4 STRUCTURE

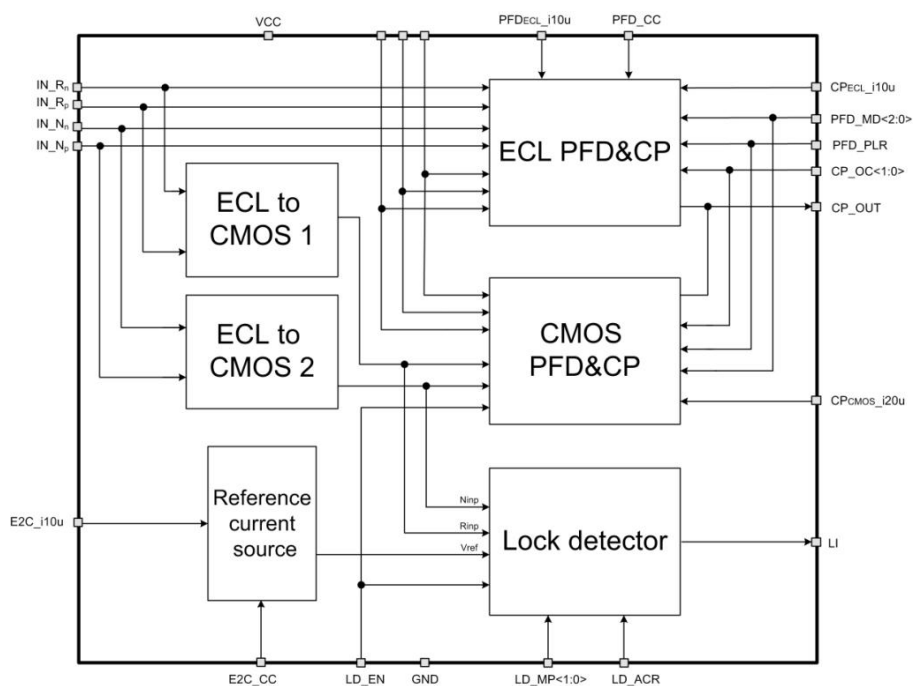
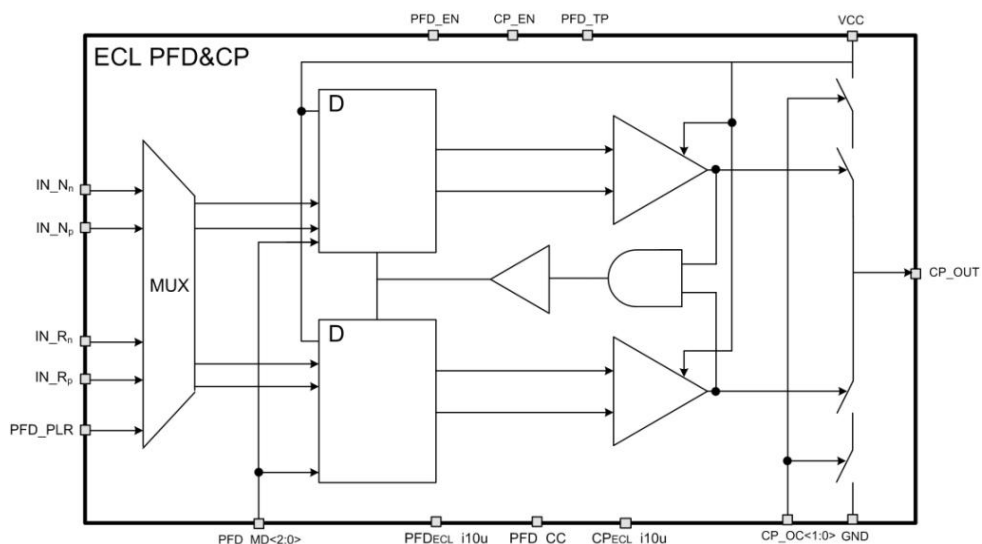
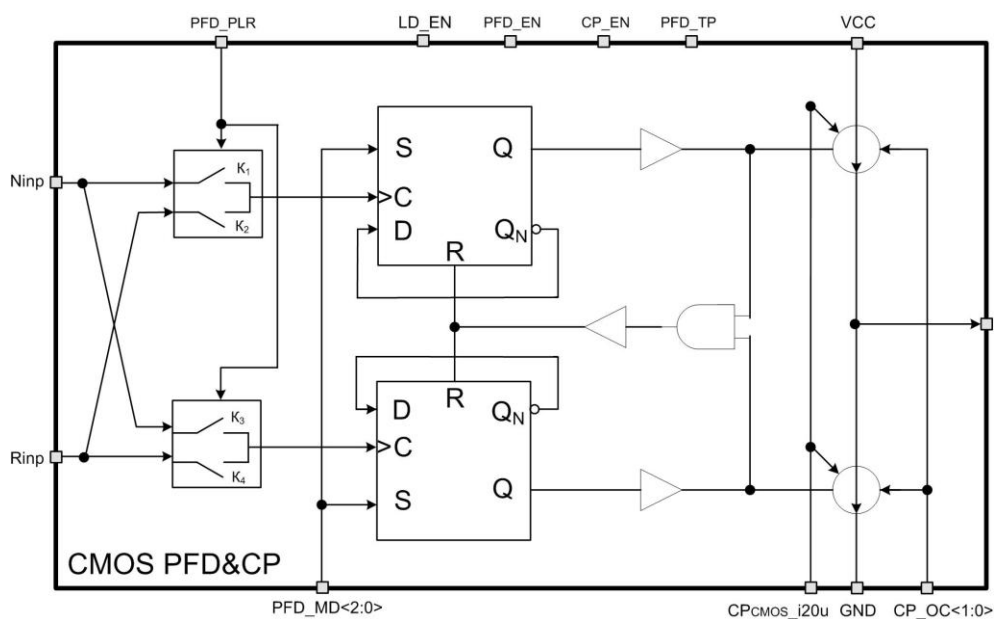


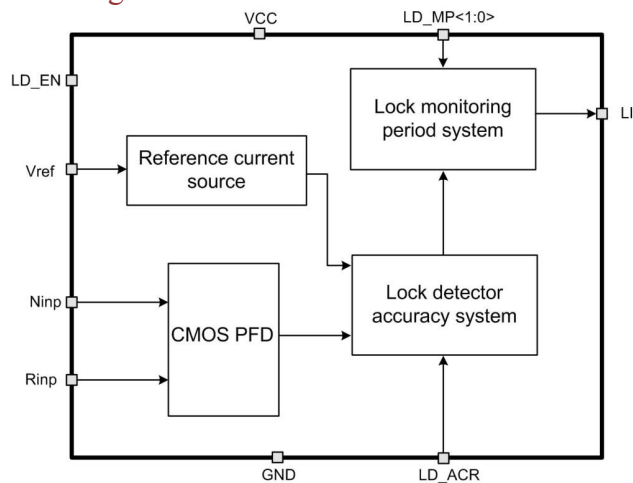
Figure 1: Phase frequency detector and charge pump structure.



**Figure 2:** ECL PFD and CP structure.



**Figure 3:** CMOS PFD and CP structure.



**Figure 4:** Lock detector structure.

## 5 PIN DESCRIPTION

Name	Direction	Description
PFD <sub>ECL</sub> _i10u	I	PFD reference current 10 $\mu$ A
CP <sub>ECL</sub> _i10u	I	Charge pump reference current 10 $\mu$ A
CP <sub>CMOS</sub> _i20u	I	Charge pump reference current 20 $\mu$ A
ECT_to_CMOS_i10u	I	ECL/CMOS converter reference current 10 $\mu$ A
IN_N <sub>p</sub>	I	PLL VCO divided signal differential input
IN_N <sub>n</sub>		
IN_R <sub>p</sub>	I	PLL reference oscillator signal differential input
IN_R <sub>n</sub>		
PFD_EN	I	PFD enable/disable
CP_EN	I	Charge pump enable/disable
LD_EN	I	Lock detector enable/disable
PFD_PLR	I	PFD polarity
PFD_CC	I	PFD current consumption control
PFD_TP	I	Charge pump type select: ECL/CMOS
CP_OC<1:0>	I	Charge pump output current control
PFD_MD<2:0>	I	Phase detector reset circuit control
E2C_CC	I	ECL/CMOS converter current consumption control
LD_MP<1:0>	I	Lock monitoring period control
LD_ACR	I	Lock detector accuracy control
CP_OUT	O	Charge pump output
LI	O	Lock indicator output
GND	IO	Ground
VCC	IO	Supply voltage

## 6 LAYOUT DESCRIPTION

Frequency-phase detector and charge pump dimensions are given in the table 1.

**Table 1:** Blocks dimensions.

Dimension	Value	Unit
Height	270	$\mu\text{m}$
Width	350	$\mu\text{m}$

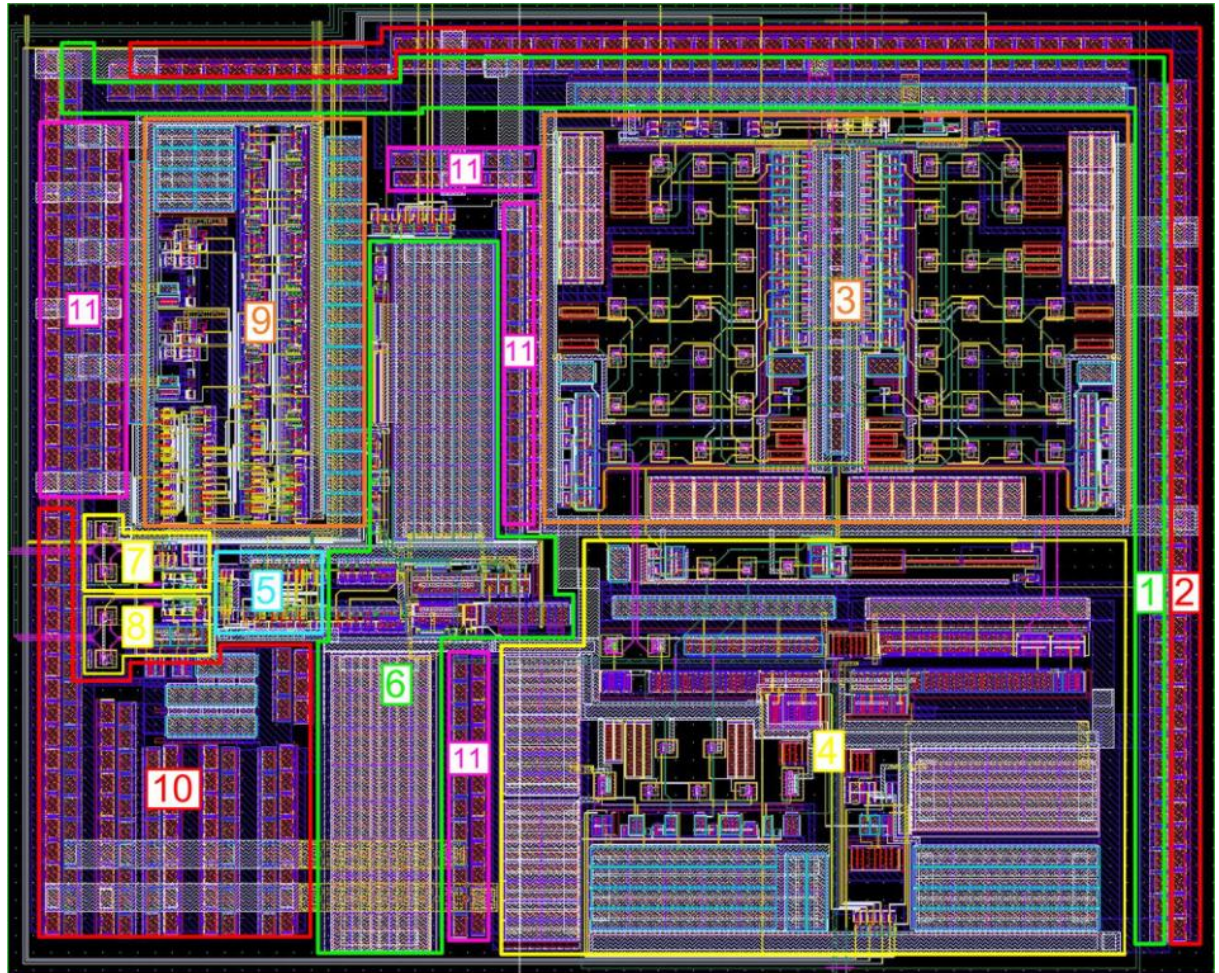


Figure 5: PFD and CP layout view.

1. Ground bus
2. Supply voltage bus
3. ECL PFD with filter capacitors
4. ECL CP with filter capacitors
5. CMOS PFD with filter capacitors
6. ECL CP with filter capacitors
7. ECL/CMOS converter of a reference oscillator signal
8. ECL/CMOS converter of VCO divided signal
9. Lock detector
10. ECL/CMOS converter of reference current source
11. Filter capacitors

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ TSMC018 SiGe  
 Status \_\_\_\_\_ Silicon proven  
 Area \_\_\_\_\_ 0.095 mm<sup>2</sup>

### 7.2 ELECTRICAL CHARACTERISTICS

#### 7.2.1 CHARACTERISTICS IN “ECL PFD&CP” OPERATING MODE

The values of electrical characteristics are specified for  $V_{cc} = 3.0 \div 3.3$  V и  $T = -40 \div +85$  °C. Typical values are at  $V_{cc} = 3.15$  V,  $T = +27$  °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	$V_{CC}$	-	3.0	3.15	3.3	V
Operating temperature range	T	-	-40	+27	+85	°C
Reference frequency	$F_{ref}$	-	-	24.84	-	MHz
Peak-to-peak voltage at the differential input	$A_{in\ p-p}$	For inputs $IN_p$ , $IN_n$ , $IN_{Rp}$ , $IN_{Rn}$	0.2	-	2.0	mV
DC operating point	$V_{op}$		$V_{cc} - 1.2$	$V_{cc}$	$V_{cc} - 0.4$	V
Output current	$I_{out}$	Preset 1	19.5	20	21	mA
		Preset 2	38.5	39	41	
		Preset 3	75	78	81	
		Preset 4	95	97	101	
PFD reset time	$t_{rst}$	Preset 5	3.5	4.2	5.0	ns
		Preset 6	3.3	3.9	4.7	
Lock monitoring period	MP	$T_{ref} = \frac{1}{F_{ref}}$	$64 \times T_{ref}$	-	$512 \times T_{ref}$	µs
Lock detector accuracy	ACR	Preset 10	5.5	6	6.5	ns
		Preset 11	9.6	11	12.4	
Supply current	$I_{cc}$	Preset 7	1.37	1.4	1.47	mA
		Preset 8	1.78	1.84	1.94	
		Preset 9	1.5	1.55	1.65	
Stand-by current	$I_{stb}$	-	1.7	2.2	287.7	nA
Input logic-level high	$V_{IH}$	For digital inputs	$0.7V_{cc}$	-	$V_{cc} + \frac{0.2}{5}$	V
Input logic-level low	$V_{IL}$		-0.25	-	0.3	V

Note:

Control signal PFD\_TP is set to “0” in “ECL PFD&CP” operating mode. CP output current is set by the control signals PFD\_TP and CP\_OC.

**Table 2:** Presets description

Presets name	Control signal values		Notes
Preset 1	PFD_TP = “0”	CP_OC<1:0> = “00”	CP output current control
Preset 2	PFD_TP = “0”	CP_OC<1:0> = “01”	
Preset 3	PFD_TP = “0”	CP_OC<1:0> = “10”	
Preset 4	PFD_TP = “0”	CP_OC<1:0> = “11”	

Table 2 (continue)

Presets name	Control signal values			Notes
Preset 5	PFD_TP = "0"	PFD_MD<2:0> = "0XX"		PFD reset time control
Preset 6	PFD_TP = "0"	PFD_MD<2:0> = "1XX"		
Preset 7	PFD_TP = "0"	PFD_CC = "0"	LD_EN = "0"	Operation mode when ECL PFD and CP extra current is disabled
Preset 8	PFD_TP = "0"	PFD_CC = "1"	LD_EN = "0"	Operation mode when ECL PFD and CP extra current is enabled.
Preset 9	PFD_TP = "0"	PFD_CC = "0"	LD_EN = "1"	Operation mode when ECL PFD and CP extra current is enabled. LD is enabled.
Preset 10	LD_ACR = "0"			Lock detector accuracy control
Preset 11	LD_ACR = "1"			

## 7.2.2 CHARACTERISTICS IN "CMOS PFD&CP" OPERATING MODE

The values of electrical characteristics are specified for  $V_{cc} = 3.0 \div 3.3$  V and  $T = -40 \div +85$  °C. Typical values are at  $V_{cc} = 3.15$  V,  $T = +27$  °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	$V_{CC}$	-	3.0	3.15	3.3	V
Operating temperature range	T	-	-40	+27	+85	°C
Reference frequency	$F_{ref}$	-	-	24.84	-	MHz
Peak-to-peak voltage at the differential input	$A_{in\ p-p}$	For inputs $IN_p, IN_{N_n}, IN_{R_p}, IN_{R_n}$	0.2	-	2.0	mV
DC operating point	$V_{op}$		$V_{cc} - 1.2$	$V_{cc}$	$V_{cc} - 0.4$	V
Output current	$I_{out}$	Preset 1	12.5	13	14	mA
		Preset 2	24.5	25	27.5	
		Preset 3	49	50	54	
		Preset 4	97	99.5	105.5	
PFD reset time	$t_{rst}$	-	1.1	1.5	2.3	ns
Lock monitoring period	MP	$T_{ref} = \frac{1}{F_{ref}}$	$64 \times T_{ref}$	-	$512 \times T_{ref}$	μs
Lock detector accuracy	ACR	Preset 7	5.5	6	6.5	ns
		Preset 8	9.6	11	12.4	
Supply current	$I_{cc}$	Preset 7	0.17	0.18	0.2	mA
		Preset 8	0.3	0.33	0.38	
Stand-by current	$I_{stb}$	-	1.7	2.2	287.7	nA
Input logic-level high	$V_{IH}$	For digital inputs	$0.7V_{cc}$	-	$V_{cc} + 0.25$	V
Input logic-level low	$V_{IL}$		-0.25	-	0.3	V

Note:

Control signal PFD\_TP is set to "1" in "CMOS PFD&CP" operating mode. CP output current is set by the control signals CP\_OC <1:0>.

**Table 3:** Presets description.

Presets name	Control signal values		Notes
Preset 1	PFD_TP = "0"	CP_OC<1:0> = "00"	CP output current control
Preset 2	PFD_TP = "0"	CP_OC<1:0> = "01"	
Preset 3	PFD_TP = "0"	CP_OC<1:0> = "10"	
Preset 4	PFD_TP = "0"	CP_OC<1:0> = "11"	
Preset 5	PFD_TP = "0"	LD_EN = "0"	Operation mode when a lock detector is disabled
Preset 6	PFD_TP = "0"	LD_EN = "1"	Operation mode when a lock detector is enabled
Preset 7	LD_ACR = "0"		Lock detector accuracy control
Preset 8	LD_ACR = "1"		

## 8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation