Phase frequency detector and charge pump

SPECIFICATION

1 FEATURES

- TSMC018 SiGe 0.18µm
- CMOS input signals
- Low disbalance of output current
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

2 APPLICATION

- Phase-locked loop synthesizer

3 OVERVIEW

Phase-frequency detector (PFD) forms control signal for VCO tuning. PFD compares phases of divided VCO signal and divided reference oscillator signal and detects phase difference. Charge pump generates pulses for loop filter.
The block is fabricated on TSMC018 SiGe 0.18µm technology.

4 STRUCTURE

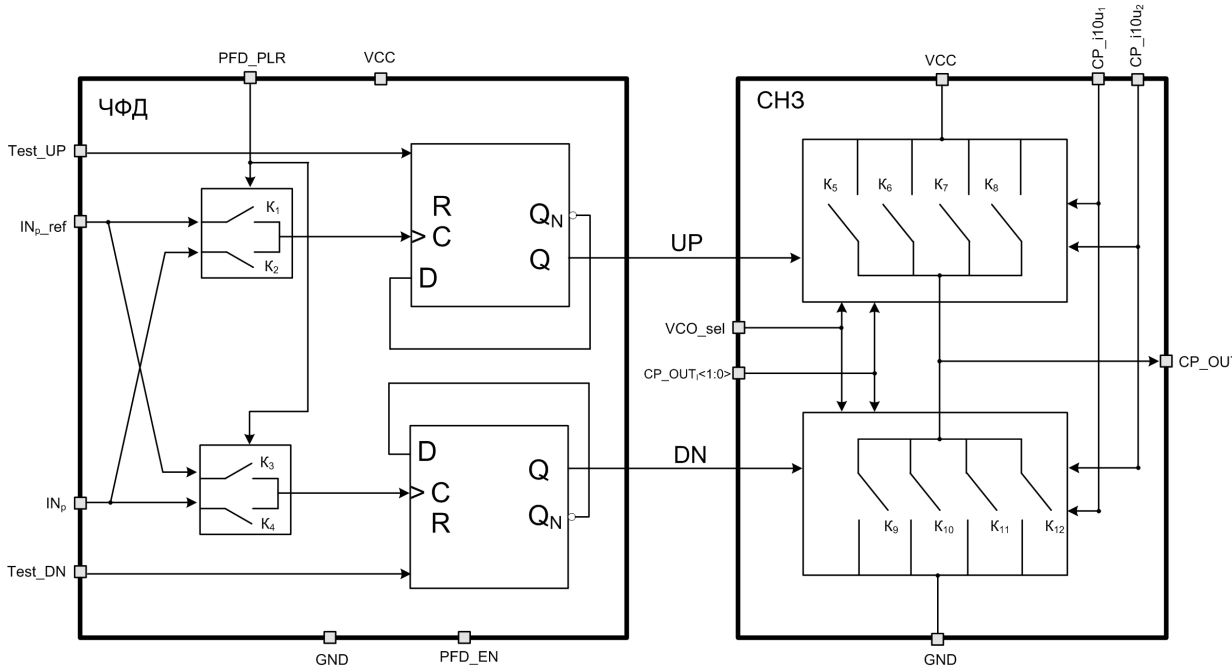

Figure 1: Phase frequency detector and charge pump structure.

5 PIN DESCRIPTION

Name	Direction	Description
CP_i20u_1	IO	CP reference current
CP_i20u_2	IO	
IN_p	I	PLL VCO divided signal input
IN_{n_ref}	I	PLL reference oscillator divided signal input
PFD_{ECL}_EN	I	PFD and CP enable/disable
PFD_{ECL}_PLR	I	PFD polarity
PFD_{ECL}_CC	I	PFD current consumption control
Test_UP	I	Enable/disable of PFD up static current test mode
Test_DN	I	Enable/disable of PFD down static current test mode
CP_OUT	IO	CP output
CP_OUT_I<1:0>	I	Output current adjustment
VCO_sel<1:0>	I	
GND	IO	Ground
VCC	IO	Supply voltage

6 LAYOUT DESCRIPTION

Frequency-phase detector and charge pump dimensions are given in the table 1.

Table 1: Blocks dimensions.

Dimension	Value	Unit
Height	139	µm
Width	108	µm

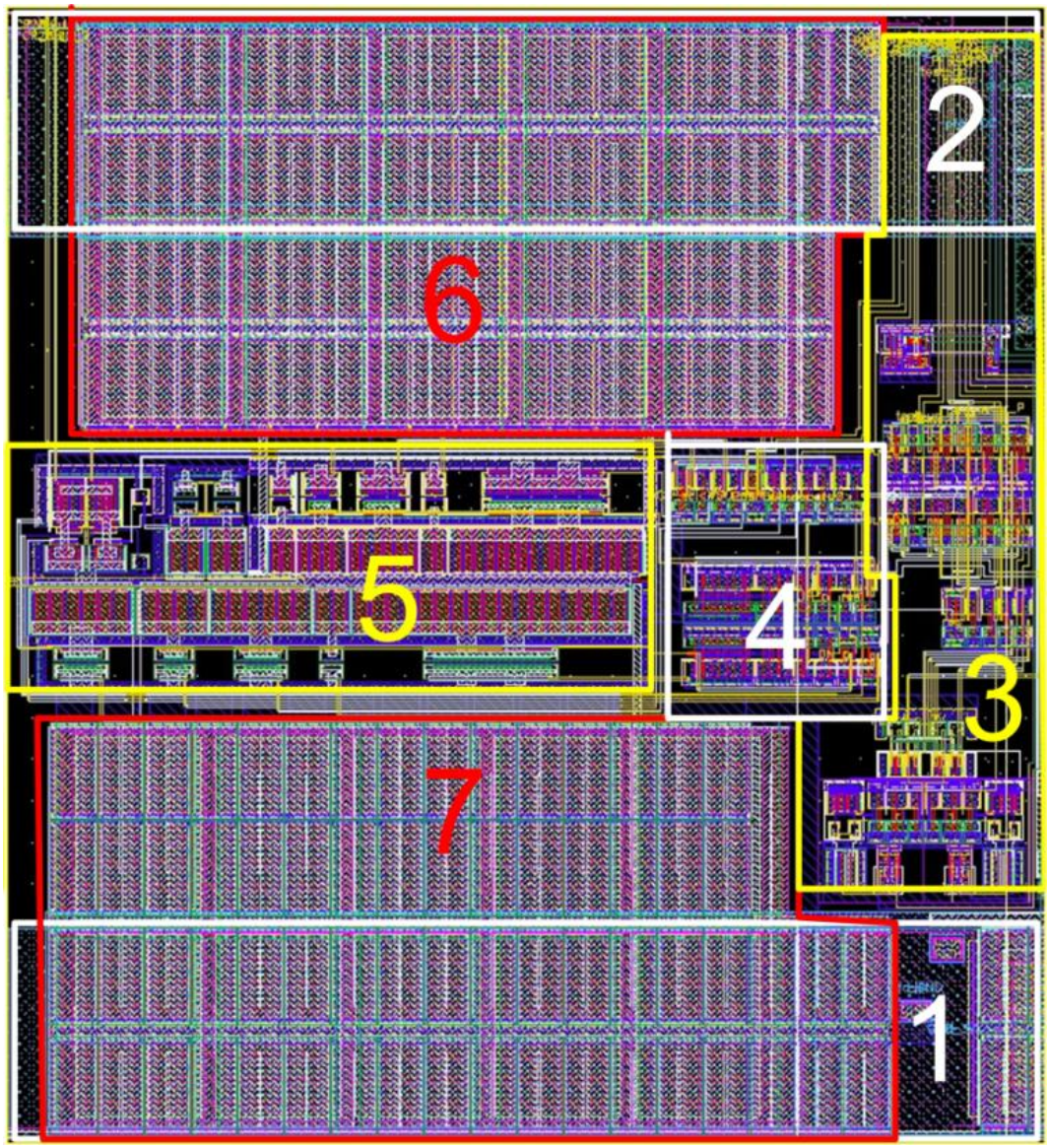

Figure 2: PFD and CP layout view.

1 Ground bus
2 Supply voltage bus
3 Phase detector
4 PFD reset circuit
5 Charge pump output stage
6 Supply voltage filter
7 Ground filter

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC018 SiGe
Status _____ silicon proven
Area _____ 0.02 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{cc} = 3.0 \div 3.6$ V и $T = -40 \div +85$ °C. Typical values are at $V_{cc} = 3.15$ V, T = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{CC}	-	3.0	3.15	3.6	V
Operating temperature range	T	-	-40	+27	+85	°C
Reference frequency	F_{ref}	-	0.1	20	25	MHz
Input amplitude	$A_{in\ p\text{-}p}$	For inputs IN_p, $IN_{p\ ref}$	$V_{cc} - 0.4$	V_{cc}	$V_{cc} + 2.4$	V
Output current	I_{out}	Preset 1	44	45	51.5	µA
		Preset 2	49.5	50	57.5	
		Preset 3	65	66	75.5	
		Preset 4	75	76.5	87.5	
		Preset 5	87.5	89	99.5	
		Preset 6	98	99.5	111.5	
		Preset 7	128.5	131	146.5	
		Preset 8	149	152	170	
		Preset 9	174	176.5	194	
		Preset 10	194	197	216.5	
		Preset 11	255.5	260	285	
		Preset 12	296	300.5	330	
		Preset 13	345.5	350	379.5	
		Preset 14	386.5	391.5	424	
		Preset 15	508	515	558	
		Preset 16	589.5	597	647	
PFD reset time	t_{rst}	-	0.74	1.07	1.87	ns
Supply current	I_{cc}	Preset 1	0.06	0.07	0.08	mA
		Preset 16	0.13	0.14	0.15	
Stand-by current	I_{stb}	Preset 16	0.25	0.67	12.5	nA
Input logic-level high	V_{IH}	For digital inputs	$0.7V_{cc}$	-	$V_{cc} + 0.25$	V
Input logic-level low	V_{IL}		-0.25	-	0.3	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation