

Phase frequency detector and charge pump

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 250 nm
- CMOS input signals
- Low disbalance of output current
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SiTerra

2 APPLICATION

- Phase-locked loop synthesizer

3 OVERVIEW

Phase-frequency detector (PFD) forms control signal for VCO tuning. PFD compares phases of divided VCO signal and divided reference oscillator signal and detects phase difference. Charge pump generates pulses to change VCO control voltage.

The block is fabricated on iHP SiGe BiCMOS 250 nm technology.

4 STRUCTURE

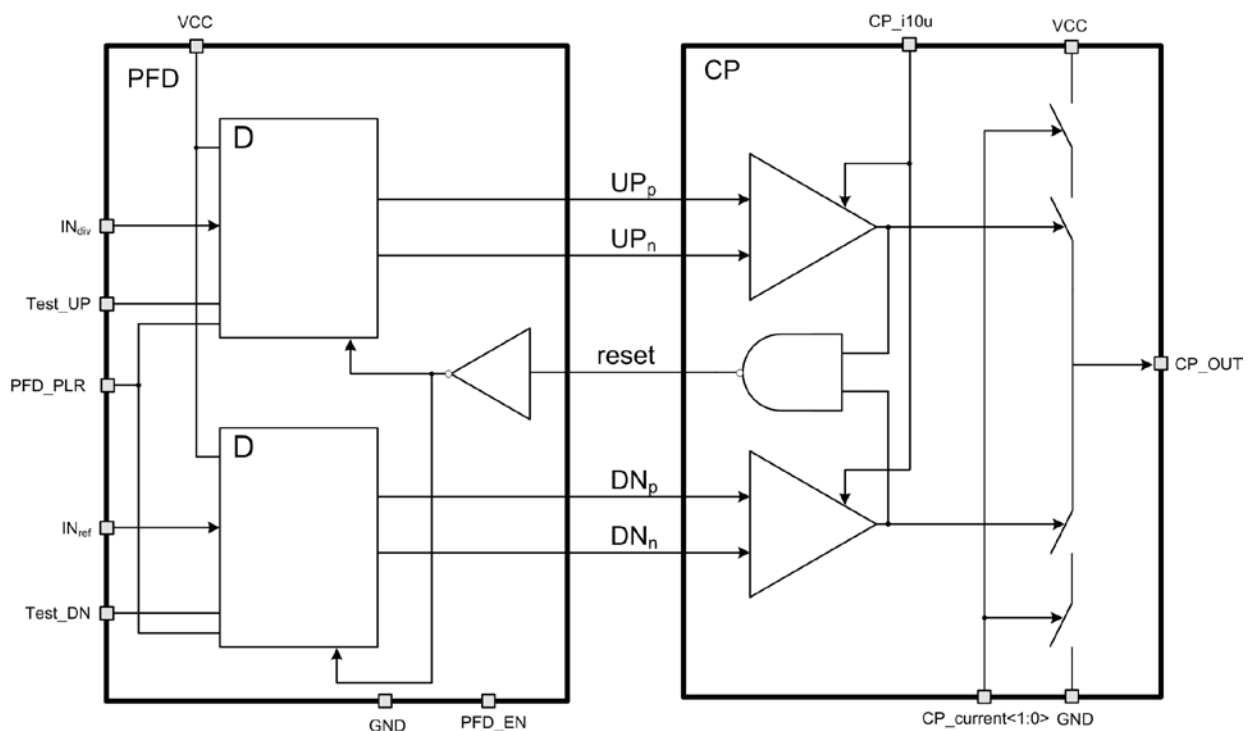


Figure 1: Phase frequency detector and charge pump structure.

5 PIN DESCRIPTION

Name	Direction	Description
CP_i10u	IO	CP reference current 10 uA
IN _{div}	I	PLL VCO divided signal input
IN _{ref}	I	PLL reference oscillator divided signal input
PFD_PLR	I	PFD polarity
PFD_EN	I	PFD and CP enable/disable
Test_UP	I	Enable/disable of PFD up static current test mode
Test_DN	I	Enable/disable of PFD down static current test mode
CP_OUT	IO	CP output
CP_current<1:0>	I	Output current adjustment
GND	IO	Ground
VCC	IO	Supply voltage

6 LAYOUT DESCRIPTION

Frequency-phase detector and charge pump dimensions are given in the table 1.

Table 1: Blocks dimensions.

Dimension	Value	Unit
Height	205	um
Width	180	um

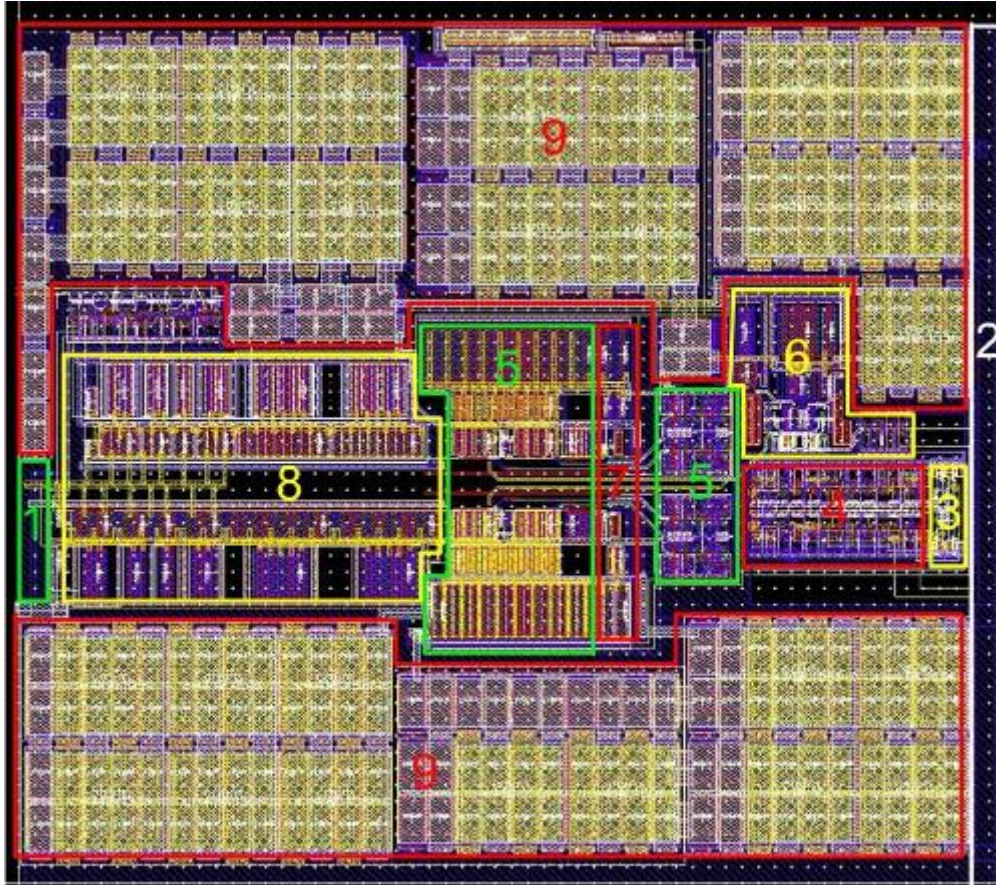


Figure 2: PFD and CP layout view.

1. Ground bus
2. Supply voltage bus
3. Polar switch
4. PFD
5. Charge pump input buffer
6. PFD reset circuit
7. Charge pump reference current source
8. Charge pump output stage
9. Filter capacitors

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 250 nm
 Status _____ silicon proven
 Area _____ 0.04 mm²

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{cc} = 2.65 \div 2.75$ V and $T_a = -60 \div +125$ °C. Typical values are at $V_{cc} = 3.15$ V, $T_a = +27$ °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	2.6	2.7	2.75	V
Operating temperature range	T_a	-	-60	+27	+125	°C
Reference frequency	F_{ref}	-	0.32	2.0	10	MHz
Peak-to-peak input voltage	$A_{in\ p-p}$	For inputs IN_{div} , IN_{ref}	$V_{cc}-0.3$	V_{cc}	$V_{cc}+0.05$	V
Charge pump output current	I_{out}	Preset 1	40	41	42	uA
		Preset 2	60.5	61.5	63	
		Preset 3	91	91.5	94	
		Preset 4	136	137	140.5	
PFD reset time	t_{rst}	-	2.5	3.0	3.7	ns
Supply current	I_{cc}	Preset 4	0.61	0.62	0.65	mA
Stand-by current	I_{stb}	Preset 4	0.3	0.05	0.25	nA
Input logic-level high	V_{IH}	For digital inputs	$0.7V_{cc}$	-	$V_{cc}+0.25$	V
Input logic-level low	V_{IL}		-0.25	-	0.3	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation