

Phase frequency detector and charge pump

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 μm
- CMOS input signals
- Low disbalance of output current
- Minimum disbalance of the charging/discharge current in loop filter capacitors
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SiTerra

2 APPLICATION

- Phase-locked loop synthesizer

3 OVERVIEW

Phase-frequency detector (PFD) forms control signal for VCO tuning. PFD compares phases of divided VCO signal and divided reference oscillator signal and detects phase difference. Charge pump generates pulses to change VCO control voltage. The CP output stage is an amplifier equalizing a buffer reference voltage of CP output current: adjustment with a loop filter voltage; and an amplifier minimizing the disbalance of the charging/discharge current in loop filter capacitors.

The block is fabricated on iHP SiGe BiCMOS 0.25 μm technology.

4 STRUCTURE

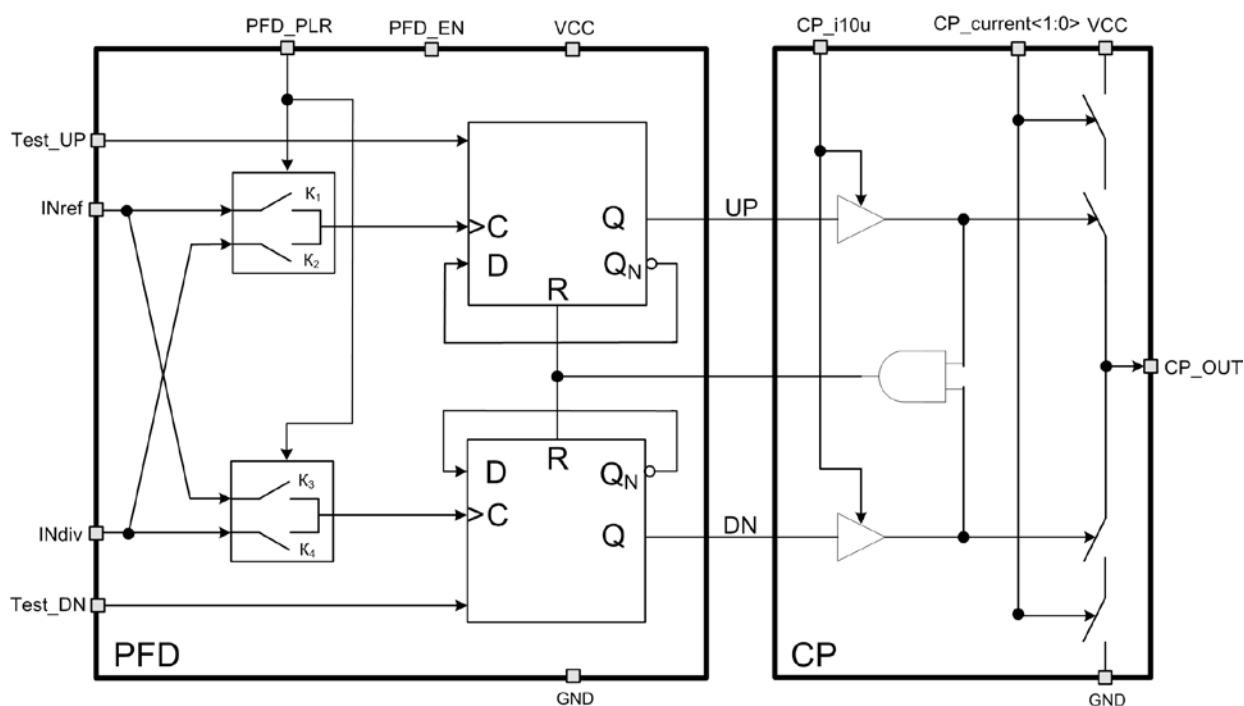


Figure 1: Phase frequency detector and charge pump structure.

5 PIN DESCRIPTION

| Name | Direction | Description |
|-------------------|-----------|---|
| CP_i10u | IO | CP reference current 10 uA |
| IN _{div} | I | PLL VCO divided signal input |
| IN _{ref} | I | PLL reference oscillator divided signal input |
| PFD_PLR | I | PFD polarity |
| PFD_RD | I | PFD reset time control |
| PFD_EN | I | PFD and CP enable/disable |
| CP_MD<3:0> | I | The control of offset and accuracy modes for output current adjustment of a loop filter |
| CP_current<1:0> | O | Output current adjustment of loop filter |
| CP_OUT | IO | CP output |
| GND | IO | Ground |
| VCC | IO | Supply voltage |

6 LAYOUT DESCRIPTION

Frequency-phase detector and charge pump dimensions are given in the table 1.

Table 1: Blocks dimensions.

| Dimension | Value | Unit |
|-----------|-------|------|
| Height | 160 | um |
| Width | 220 | um |

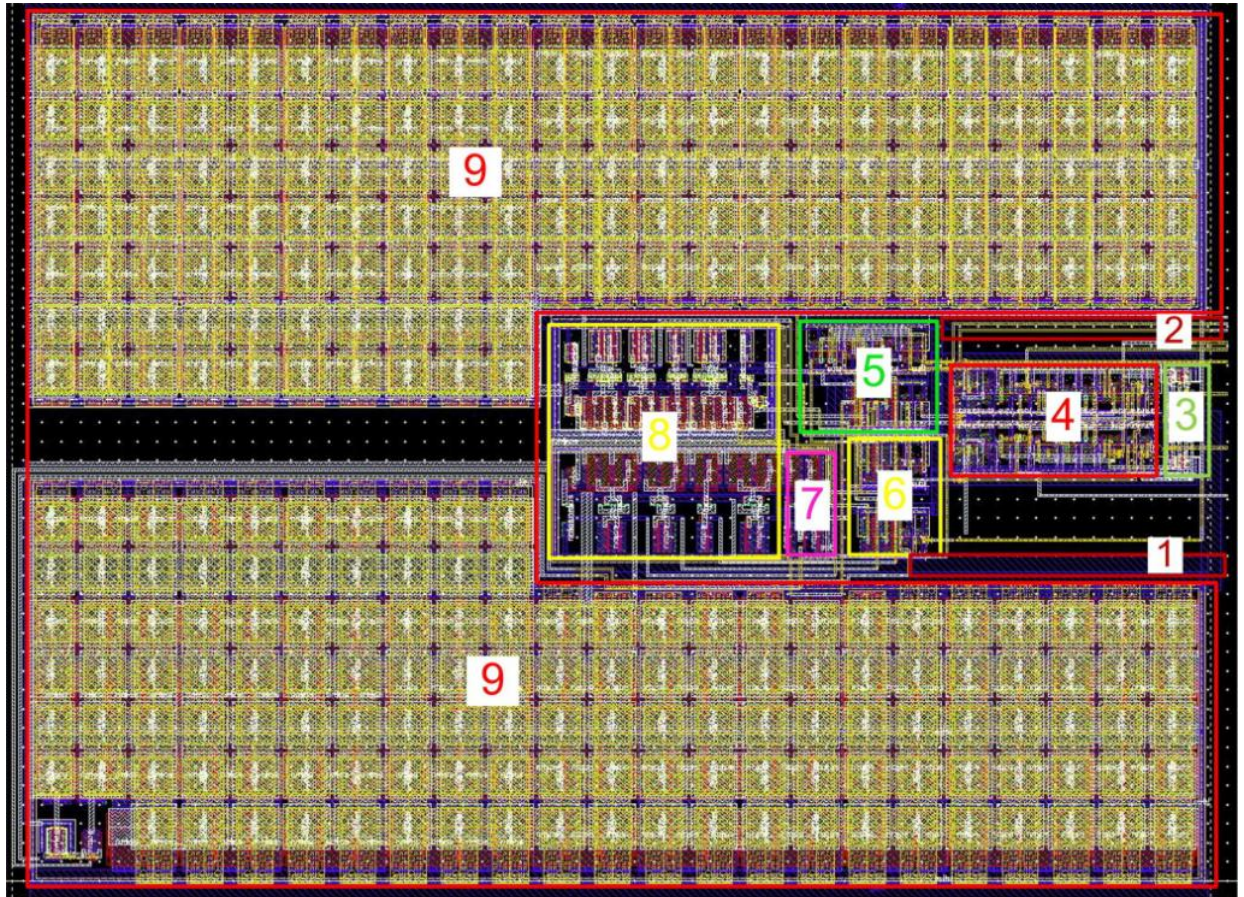


Figure 2: PFD and CP layout view.

1. Ground bus
2. Supply voltage bus
3. PFD polarity switch circuit
4. PFD
5. Charge pump input buffer
6. PFD reset circuit
7. Charge pump reference current source.
8. Charge pump output stage
9. Filter capacitors

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.25 um
 Status _____ silicon proven
 Area _____ 0.035 mm²

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{cc} = 2.65 \div 2.75$ V and $T_a = -60 \div +125$ °C. Typical values are at $V_{cc} = 3.15$ V, $T_a = 27$ °C, unless otherwise specified.

| Parameter | Symbol | Condition | Value | | | Unit |
|-----------------------------|---------------|------------------------------------|--------------|----------|---------------|------|
| | | | min | typ | max | |
| Supply voltage | V_{cc} | - | 2.6 | 2.7 | 2.75 | V |
| Operating temperature range | T_a | - | -60 | 27 | 125 | °C |
| Reference frequency | F_{ref} | - | - | 24.84 | - | MHz |
| Peak-to-peak input voltage | $A_{in\ p-p}$ | For inputs IN_{div} , IN_{ref} | $V_{cc}-0.3$ | V_{cc} | $V_{cc}+0.05$ | V |
| Charge pump output current | I_{out} | Preset 1 | 41 | 41.5 | 42 | uA |
| | | Preset 2 | 61.5 | 62 | 63 | |
| | | Preset 3 | 92.5 | 93.5 | 94 | |
| | | Preset 4 | 140 | 141.5 | 142 | |
| PFD reset time | t_{rst} | - | 1.4 | 2.0 | 3.1 | ns |
| Supply current | I_{cc} | Preset 4 | 23.5 | 23.1 | 23.2 | uA |
| Stand-by current | I_{stb} | Preset 4 | 2.5 | 3.0 | 5.0 | nA |
| Input logic-level high | V_{IH} | For digital inputs | $0.7V_{cc}$ | - | $V_{cc}+0.25$ | V |
| Input logic-level low | V_{IL} | | -0.25 | - | 0.3 | V |

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation