Phase frequency detector and charge pump

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Input CMOS signal
- Low output current disbalance
- High lock detector accuracy

2 APPLICATION

- Phase-locked loop synthesizer

3 OVERVIEW

Phase-frequency detector (PFD) is used to form a control signal VCO tuning. PFD compares phases of a divided VCO signals and a divided reference oscillator signals and detects phase difference. Charge pump generates pulses to change VCO control voltage. This structure includes of ECL charge pump and CMOS charge pump.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

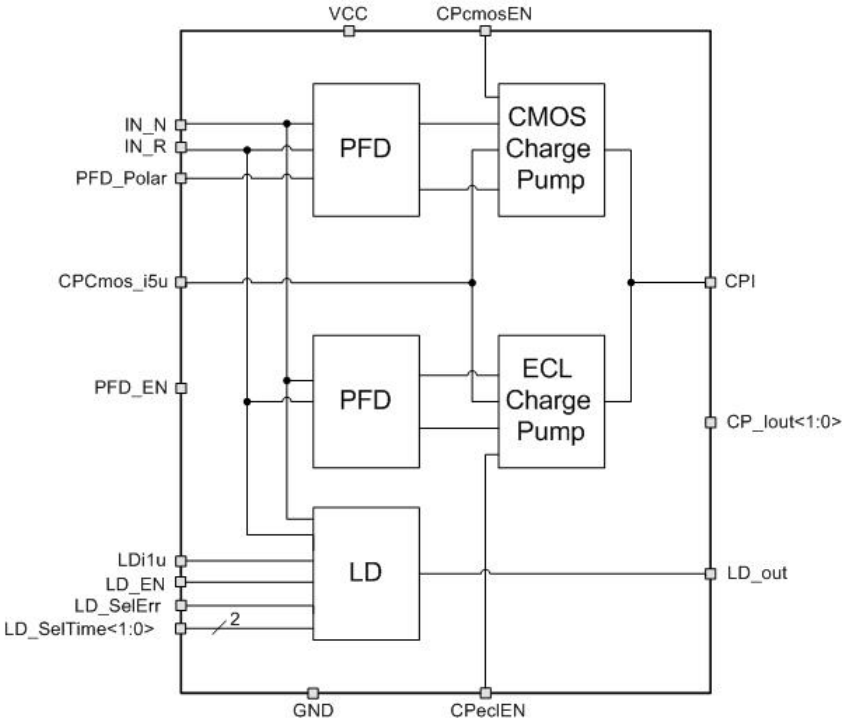

Figure 1: Phase frequency detector and charge pump structure.

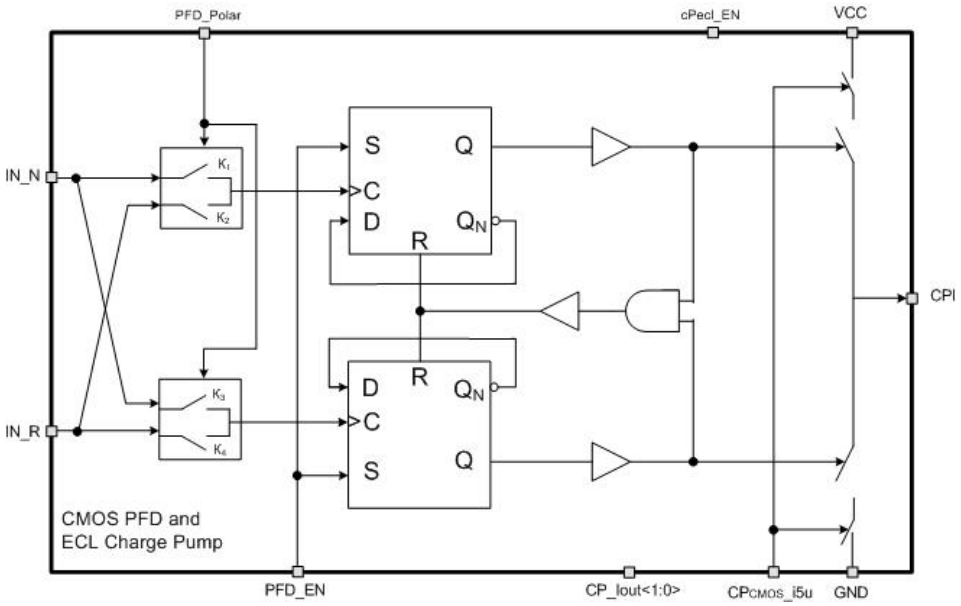

Figure 2: CMOS PFD and ECL charge pump structure.

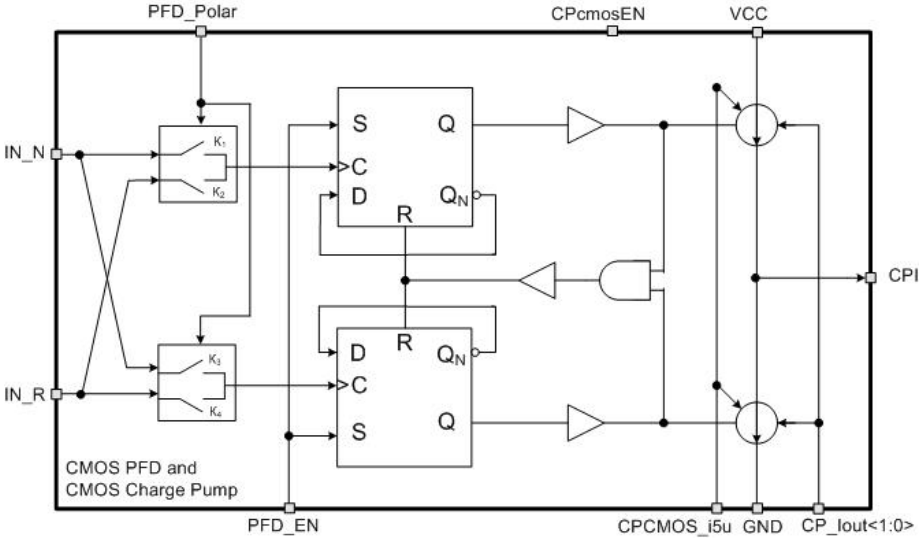

Figure 3: CMOS PFD and CMOS charge pump structure

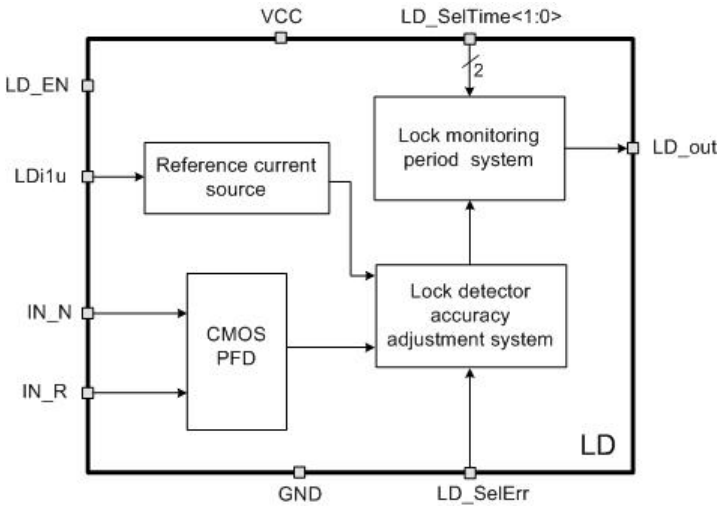

Figure 4: Lock detector structure.

5 PIN DESCRIPTION

Name	Direction	Description
CPcmos_i5u	I	CMOS charge pump reference current (5 uA)
CPecl_i5u	I	Charge pump reference current (5 uA)
IN_N	I	CMOS PLL VCO divided signal input
IN_R	I	CMOS PLL reference oscillator signal input
LD_SelErr	I	Detection accuracy adjustment
PFD_Polar	I	PFD polarity
LD_EN	I	Lock detector enable/disable
PFD_EN	I	PFD enable/ disable
CPcmosEN	I	CMOS charge pump enable/disable
CPeclEN	I	ECL charge pump enable/disable
LD_SelTime<1:0>	I	Detection period adjustment
CP_Iout<1:0>	I	Charge pump output current control
CPI	O	Charge pump output
LD_out	O	Lock detector output
VCC	O	Supply voltage
GND	O	Ground

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	245.67	um
Width	286.14	um

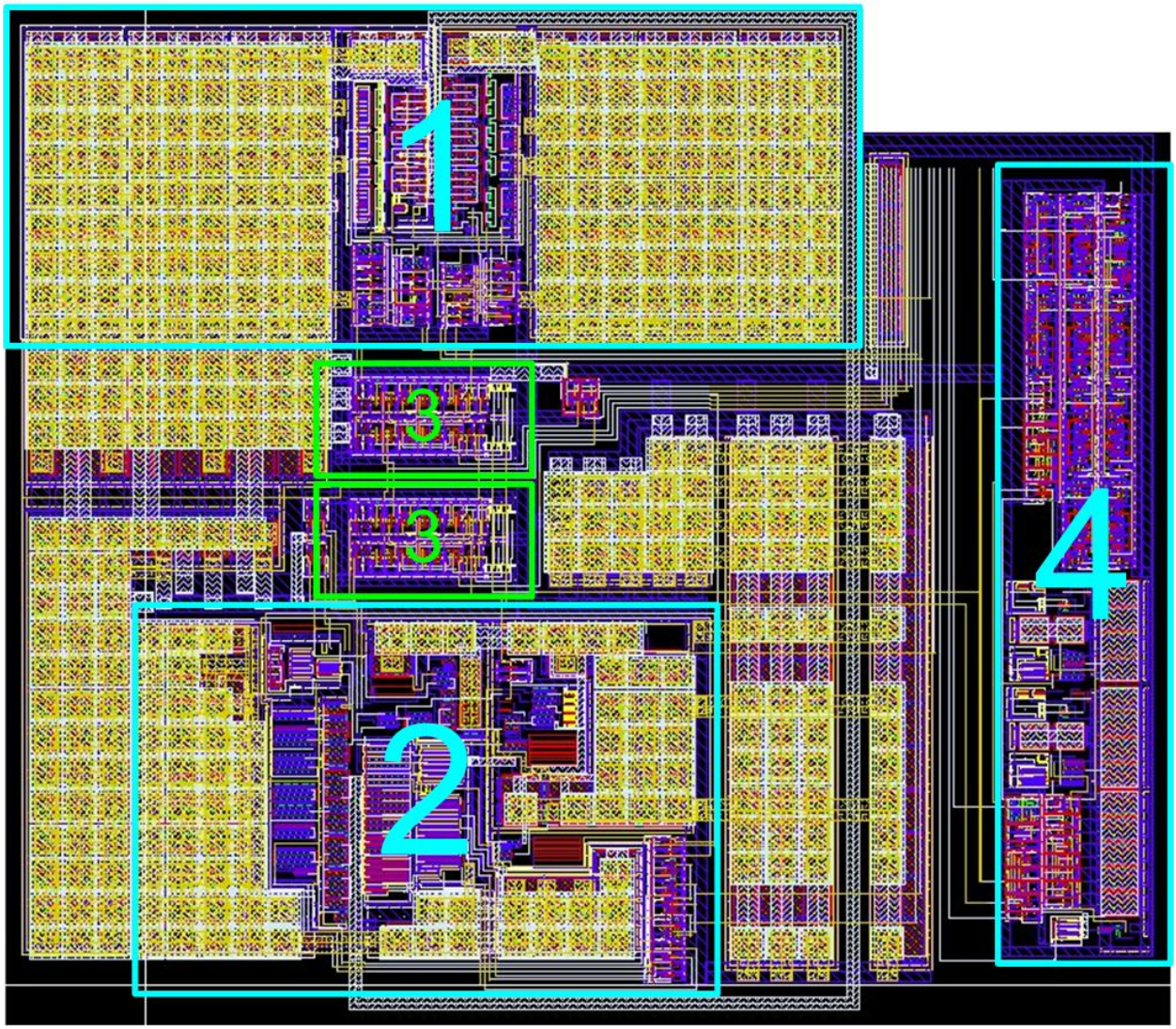

Figure 5: Device layout view.

1. CMOS charge pump
2. ECL charge pump
3. CMOS PFD
4. Lock detector

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.25 um
Status _____ silicon proven
Area _____ 0.07 mm^2

7.2 ELECTRICAL CHARACTERISTICS

7.2.1 CHARACTERISTICS AT WORK OF CMOS PFD AND CMOS CHARGE PUMP

The values of electrical characteristics are specified for V_{cc} = 1.7 ÷ 2.3 V and T_a = -45 ÷ +85 °C. Typical values are at V_{cc} = 2.2 V and T_a = +27° C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	1.7	2.2	2.3	V
Operating temperature range	T_a	-	-45	27	85	ºC
Reference frequency	F	-	-	100	-	kHz
Output voltage	V_{out}	-	0.14	0.88	1.58	V
Charge pump output current	I_{out}	Preset 1	40	41	43	uA
		Preset 2	60	61	65	
		Preset 3	90	91	97	
		Preset 4	135	137	145	
PFD reset time	t_{rst}	-	6.42	8.18	9.15	ns
Lock monitoring time	MP	-	0.64	-	5.2	ms
Lock detector accuracy	Serr	Preset 5	46	55	76	ns
		Preset 6	92	110	152	
Current consumption in an active mode	I_{cc}	-	77.3	80.4	88	uA
Current consumption in a standby mode	I_{stb}	-	0.37	0.61	4.32	nA
Input logic-high level	V_{IH}	For digital inputs	$0.7V_{cc}$	-	V_{cc}+0.25	V
Input logic-low level	V_{IL}		-0.25	-	0.3	V

Table 2: Preset description.

Preset	Control signal	Description
Preset 1	CP_Iout="00"	Charge pump output current adjustment
Preset 2	CP_Iout="01"	
Preset 3	CP_Iout="10"	
Preset 4	CP_Iout="11"	
Preset 5	LD_SelErr="0"	Lock detector accuracy adjustment
Preset 6	LD_SelErr="1"	

7.2.2 CHARACTERISTICS AT WORK OF CMOS PFD AND ECL CHARGE PUMP

The values of electrical characteristics are specified for V_{cc} = 1.7 ÷ 2.3 V and T_a = -45 ÷ +85 °C. Typical values are at V_{cc} = 2.2 V and T_a = +27° C, unless otherwise specified.

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8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation