CMOS charge pump

SPECIFICATION

1 FEATURES

- AMS035 BiCMOS 0.35 um technology
- Adjustable output current
- Differential current switches mode
- Single-ended mode with reduced current consumption
- Input frequency up to 100 MHz
- Portable to other technologies (upon request)

2 APPLICATION

- Phase-locked loop synthesizer

3 OVERVIEW

Charge pump (CP) is a switched current sources controlled by phase-frequency detector which inject or remove some charge to increase or decrease VCO control voltage depended on phase difference between reference frequency and divided VCO frequency.
The block is fabricated on AMS035 BiCMOS 0.35 um technology.

4 STRUCTURE

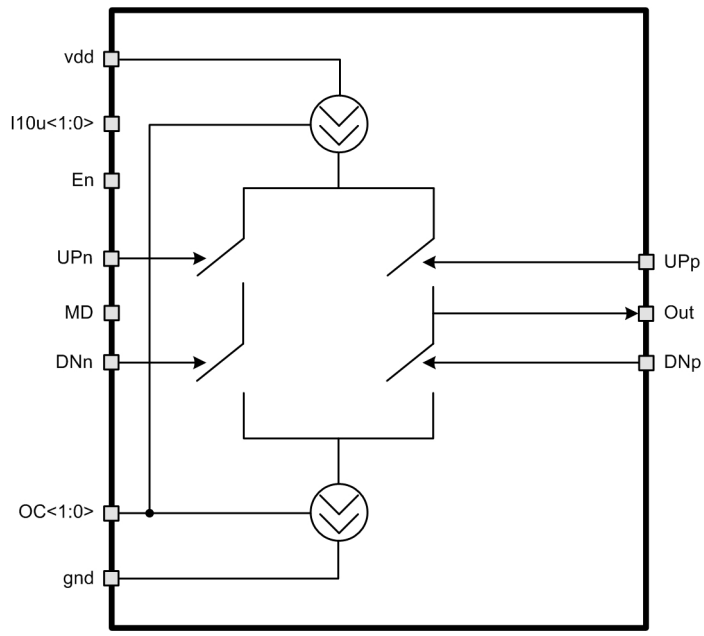

Figure 1: CMOS charge pump structure.

5 PIN DESCRIPTION

Name	Direction	Description
OC<1:0>	I	CP output current selection
En	I	Enable/disable charge pump
MD	I	Charge pump mode selection
UPp	I	Analog differential increase output voltage signal
UPn	I	
DNp	I	Analog differential decrease output voltage signal
DNn	I	
I10u<1:0>	I	Reference current (10 uA)
Out	O	Charge pump output
vdd	IO	Supply voltage
gnd	IO	Ground

6 LAUOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	215	µm
Width	315	µm

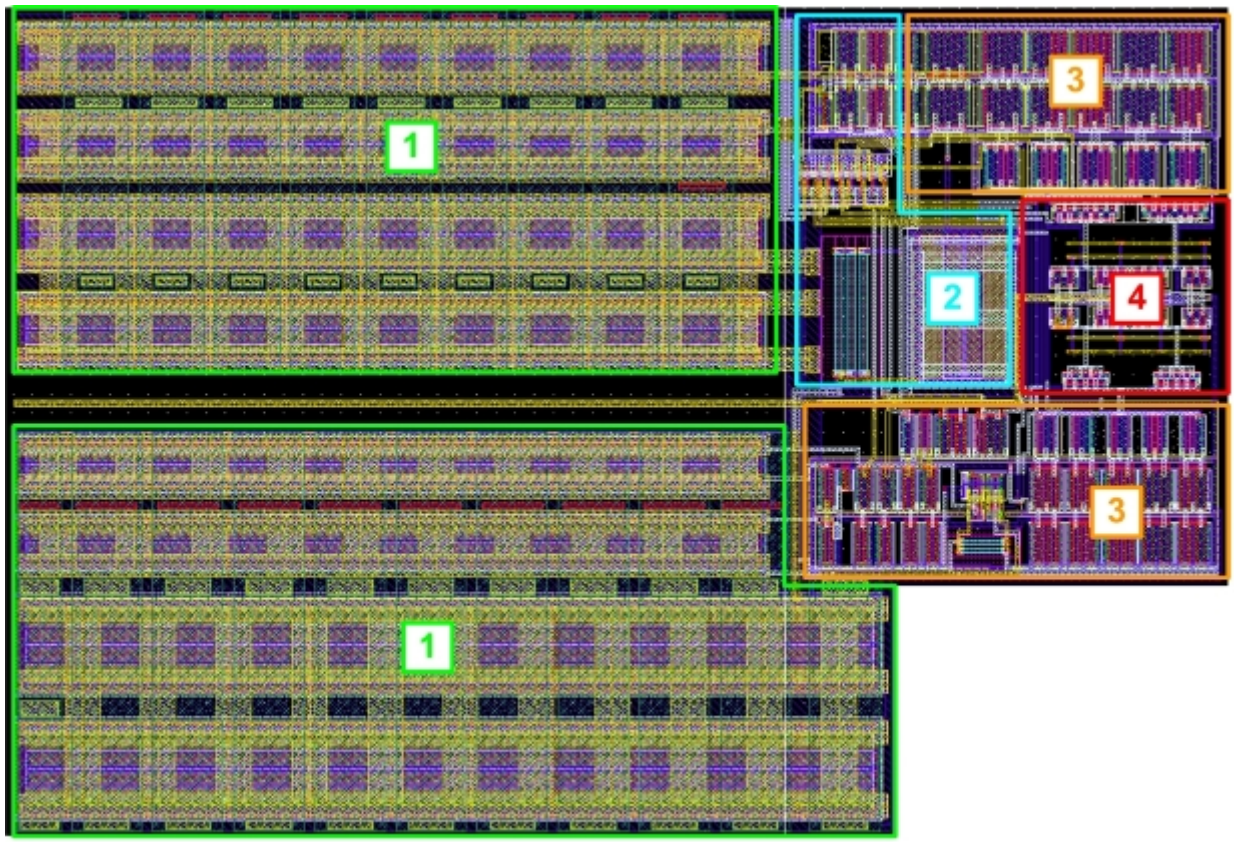

Figure 2: Charge pump layout view.

1. Filter capacitors
2. Voltage repeater
3. Current source
4. Analog switches

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology AMS035 BiCMOS 0.35 um
Status silicon proven
Area 0.063 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.6 ÷ 3.15 V, T = -40 ÷ +85 °C. Typical values are at V_{cc} = 2.7 V and T = +27° C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	2.6	2.7	3.15	V
Operating temperature range	T	-	-40	27	85	°C
Input signal frequency	F_{max}	-	-	-	100	MHz
Source current	$I_{out\ up}$	OC<1:0>=”00” - 20 uA	19.2	20.4	21.1	uA
		OC<1:0>=”01” - 40 uA	36.6	38.7	40	
		OC<1:0>=”10” - 80 uA	71.2	75.3	77.8	
		OC<1:0>=”11” -100 uA	88.6	93.6	96.7	
Sink current	$I_{out\ dn}$	OC<1:0>=”00” - 20 uA	19.4	20	20.4	uA
		OC<1:0>=”01” - 40 uA	38	39.1	39.9	
		OC<1:0>=”10” - 80 uA	75.3	77.3	78.8	
		OC<1:0>=”11” -100 uA	93.9	96.5	98.3	
Working output voltage range	V_{out}	-	0.4	-	V_{cc}-0.4	V
Supply current	I_{dd}	-	-	0.06	-	mA
Stand-by current	I_{st}	-	-	-	1	nA
Input logic-level high	V_{OH}	-	0.9V_{cc}	-	V_{cc}	V
Input logic-level low	V_{OL}	-	-0.2	0	0.2	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

1. From version 1.0:
   - Section “Technical characteristics” (refer to page 4)