Phase frequency detector and charge pump

SPECIFICATION

1 FEATURES

- AMS035 BiCMOS 0.35 µm
- Input signals with low amplitude
- Low disbalance of output current
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

2 APPLICATION

- Phase-locked loop synthesizer

3 FUNCTIONAL DESCRIPTION

Phase-frequency detector (PFD) forms control signal for VCO tuning. PFD compares phases of divided VCO signal and divided reference oscillator signal and detects phase difference. Charge pump generates pulses for loop filter.
The block is fabricated on AMS035 BiCMOS 0.35 µm technology.

4 STRUCTURE

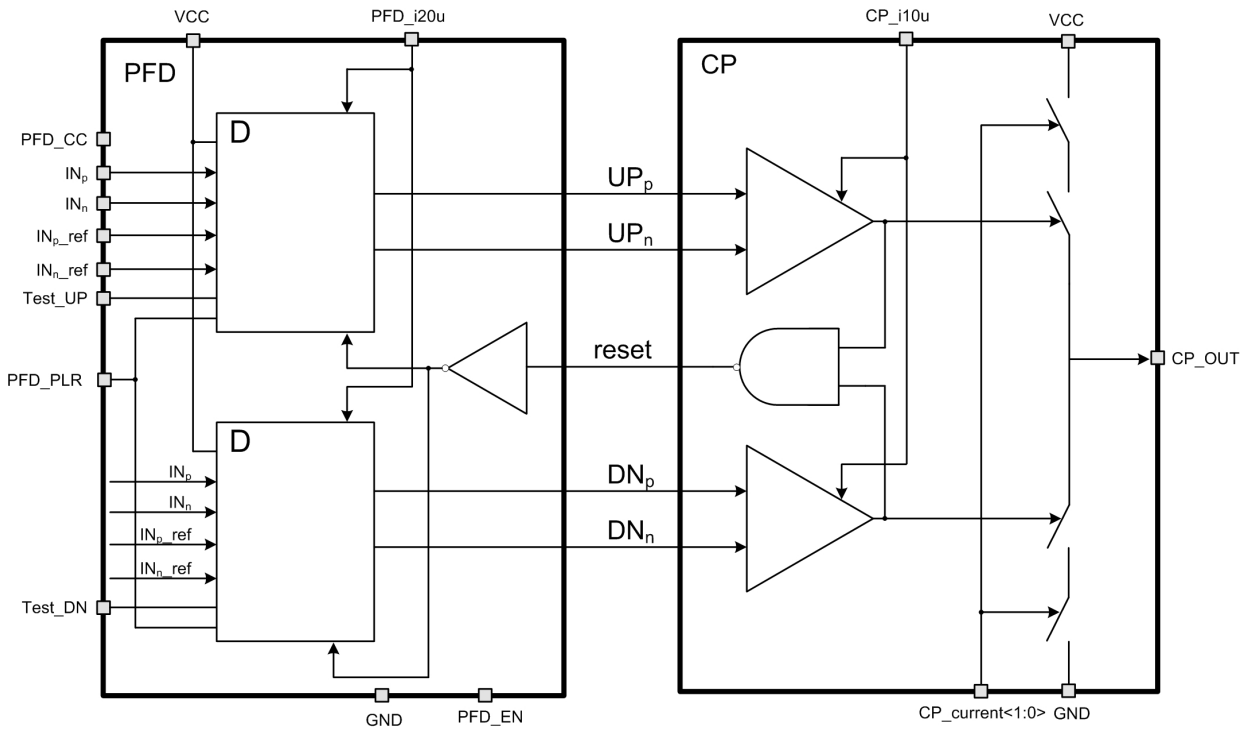

Figure 1: Phase frequency detector and charge pump structure.

5 PIN DESCRIPTION

Name	Direction	Description
PFD_i20u	IO	PFD reference current
CP_i10u	IO	Charge pump reference current
IN_p	I	PLL VCO divided signal differential input
IN_n		
IN_p_ref	I	PLL reference oscillator signal differential input
IN_n_ref		
PFD_EN	I	PFD and charge pump enable/disable
PFD_PLR	I	PFD polarity
PFD_CC	I	PFD current consumption control
Test_UP	I	Enable/disable of PFD up static current test mode
Test_DN	I	Enable/disable of PFD down static current test mode
CP_current<1:0>	I	Output current adjustment
CP_OUT	O	Charge pump output
GND	IO	Ground
VCC	IO	Supply voltage

6 LAYOUT DESCRIPTION

Frequency-phase detector and charge pump dimensions are given in the table 1.

Table 1: Blocks dimensions.

Dimension	Value	Unit
Height	316	µm
Width	500	µm

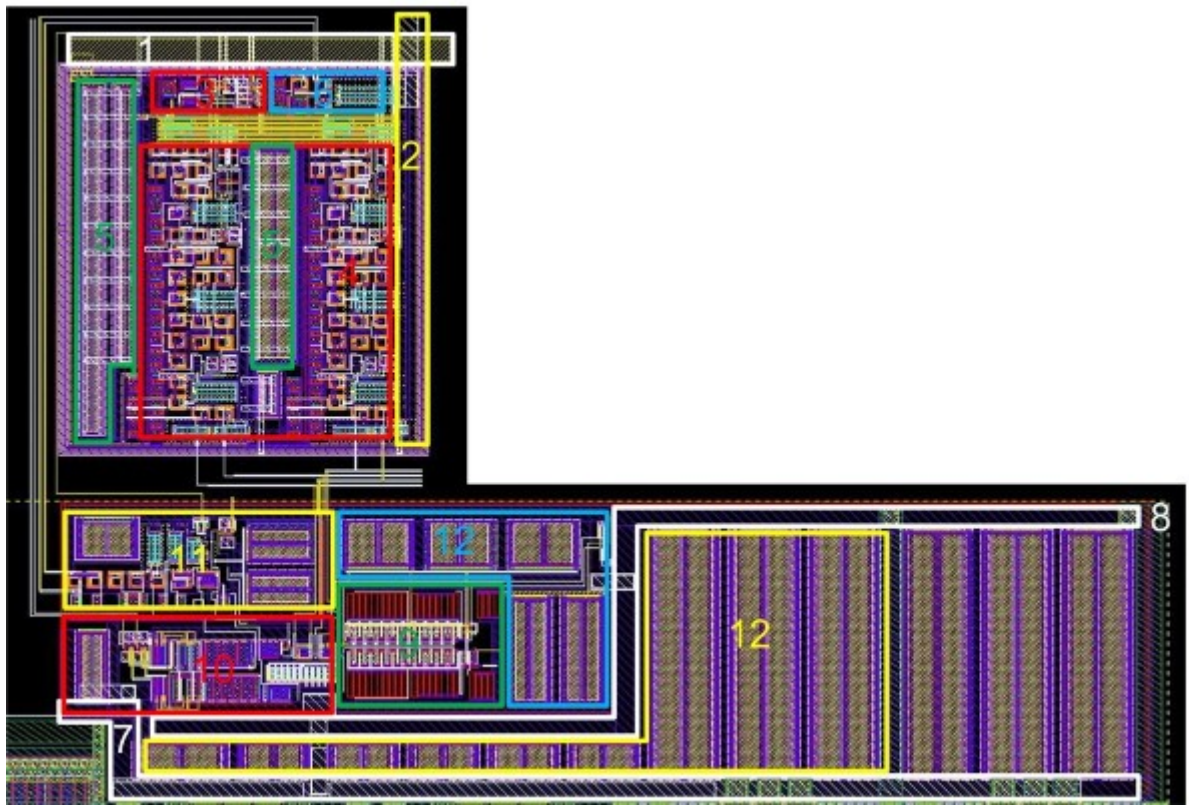

Figure 2: PFD and CP layout view.

1 PFD ground bus
2 PFD supply voltage bus
3 PFD input buffer
4 PFD triggers
5 PFD filter capacitors
6 PFD reset circuit
7 Charge pump ground bus
8 Charge pump supply voltage bus
9 Charge pump input buffer
10 Charge pump output stage
11 Signal former for phase detector reset circuit
12 Charge pump filter capasitors

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ AMS035 BiCMOS 0.35
Status _____ Silicon proven
Area _____ 0.101 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 3.0 ÷ 3.3 V и T = -40 ÷ +85 °C. Typical values are at V_{cc} = 3.15 V, T = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{CC}	-	3.0	3.15	3.3	V
Operating temperature range	T	-	-40	+27	+85	°C
Reference frequency	F_{ref}	-	-	24.84	-	MHz
Peak-to-peak voltage at the differential input	$A_{in\ p\text{-}p}$	For inputs IN_p, IN_n, IN_p_ref и IN_n_ref	0.2	-	2.0	V
DC operating point	V_{op}		V_{cc} – 1.2	-	V_{cc} – 0.2	V
Output current	I_{out}	Preset 1	19.1	19.3	20.6	µA
		Preset 2	36.8	37.4	39.6	
		Preset 3	71.4	73.0	77.4	
		Preset 4	88.7	90.7	96.3	
PFD reset time	t_{rst}	-	2.1	2.69	3.5	ns
Supply current	I_{cc}	-	1.28	1.4	1.53	mA
Stand-by current	I_{stb}	-	0.6	0.75	353.5	nA
Input logic-level high	V_{IH}	For digital inputs	0.7V_{cc}	-	V_{cc} + 0.25	V
Input logic-level low	V_{IL}		-0.25	-	0.3	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation