Phase-frequency detector in ECL logic

SPECIFICATION

1 FEATURES

- AMS035 BiCMOS 0.35 µm
- Differential structure
- Ability to work with VCOs with both positive and negative frequency dependence of the control voltage
- Input frequencies up to 100MHz
- Only-up/only-down test modes
- External reset circuit
- Portable to other technologies (upon request)

2 APPLICATION

- Phase-locked loop synthesizer

3 OVERVIEW

The phase-frequency detector (PFD) consists of 2 D-trigger with reset from external circuit, performed in ECL logic and multiplexer, which allow to switch the input signals to the corresponding inputs.
The block is fabricated on AMS035 BiCMOS 0.35 µm technology.

4 STRUCTURE

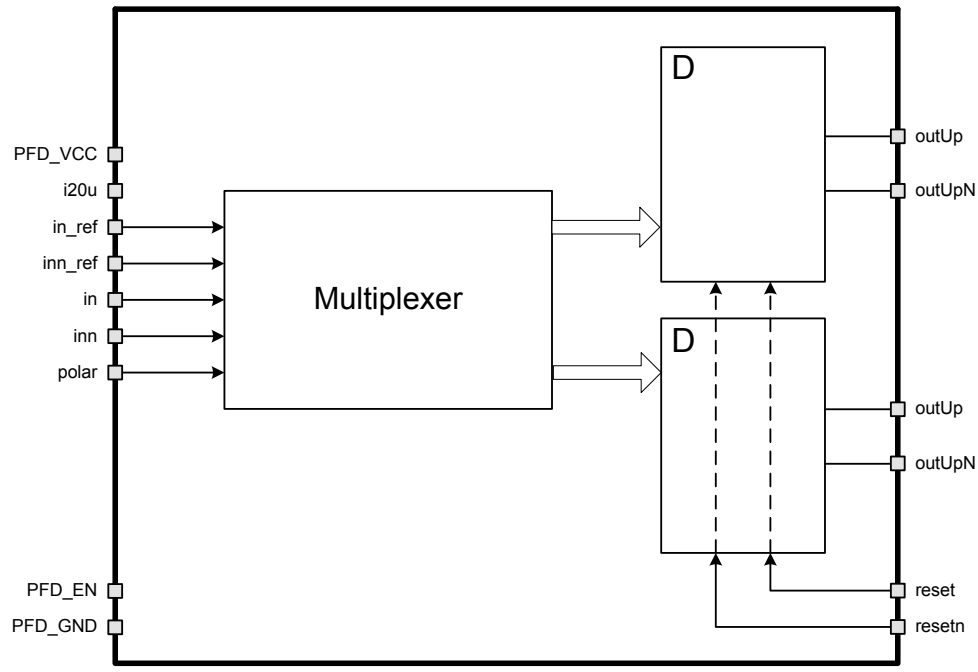

Figure 1: Phase-frequency detector in ECL logic structure

5 PIN DESCRIPTION

Name	Direction	Description
PFD_EN	I	PFD enable/disable
i20u	I	Reference current 20 µA
polar	I	PFD polarity
in	I	VCO divided signal differential ECL input
inn		
in_ref	I	Reference oscillator signal differential ECL input
inn_ref		
reset	I	PFD reset signal analog differential input
resetn		
outUp	O	Differential output signal for increase control voltage
outUpN		
outDn	O	Differential output signal for decrease control voltage
outDnP		
PFD_VCC	IO	Supply voltage
PFD_GND	IO	Ground

6 LAYOUT DESCRIPTION

Frequency-phase detector dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	165	µm
Width	175	µm

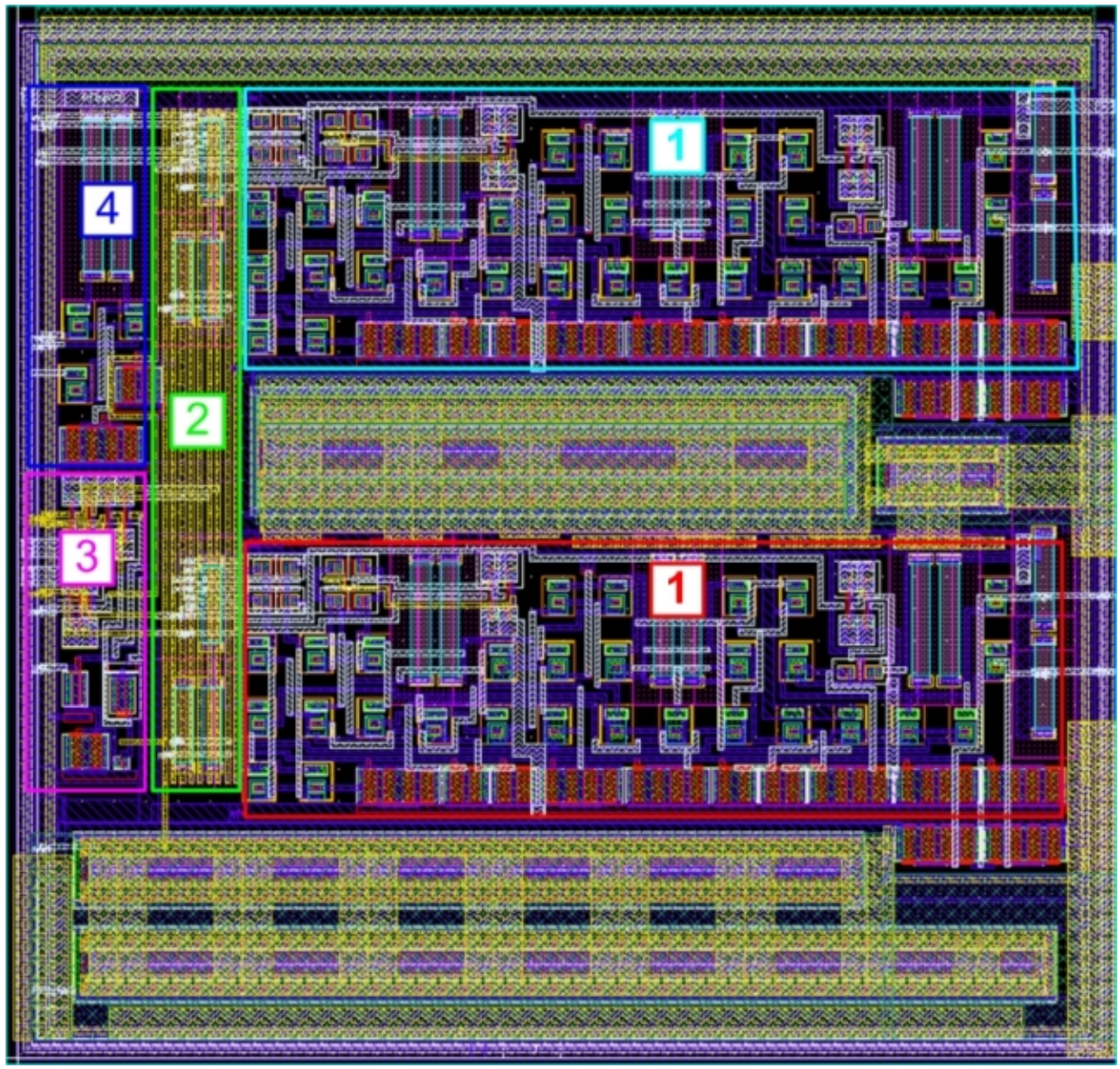

Figure 2: ECL PFD structure

1. PFD D-trigger
2. Multiplexer
3. Logic
4. PFD reset signal input

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology AMS035 BiCMOS 0.35 µm
Status silicon proven
Area 0.029mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.5 ÷ 3.6 V, T = -40 ÷ +85 °C. Typical values are at V_{cc} = 2.7 V, T = +27° C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	2.5	2.7	3.6	V
Operating temperature range	T	-	-40	27	85	°C
Input signal frequency	F_{max}	-	-	-	100	MHz
Peak-to-peak input voltage	$A_{in\ p\text{-}p}$	At differential input	0.3	0.4	0.8	V
In-phase component signal input	$A_{in\ dc}$	V_{cc}=2.7 V	1.6	1.8	V_{cc} – 0.6	V
Peak-to-peak output voltage	$A_{out\_p\text{-}p}$	At differential output	0.4	0.6	0.8	V
In-phase component signal output	$A_{out\ dc}$	V_{cc}=2.7 V	V_{cc} – 1.7	V_{cc} – 1.4	V_{cc} – 1.1	V
Supply current	I_{dd}	-	-	0.9	0.95	mA
Stand-by current	I_{st}	-	-	-	40	nA
Input logic-level high	V_{IH}	For digital inputs	0.9 V_{cc}	-	V_{cc}	V
Input logic-level low	V_{IL}		-0.2	0	0.2	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

1. From version 1.0:
   - Section “Technical characteristics” (refer to page 4)