Phase-frequency detector in CMOS logic

SPECIFICATION

1 FEATURES

- AMS035 BiCMOS 0.35 µm
- Ability to work with VCOs with both positive and negative frequency dependence of the control voltage
- Input frequencies up to 100 MHz
- Differential CMOS output signal
- CMOS output signal for lock detector
- Built-in reset delay circuit

2 APPLICATION

- Phase-locked loop synthesizer

3 OVERVIEW

The phase-frequency detector (PFD) consists of a signal level converter from differential reduced swing ECL to single-ended full swing CMOS signal and two D-flip-flops with reset, made in CMOS logic. Multiplexer allow to switch the input signals to the corresponding inputs. The block is fabricated on AMS035 BiCMOS 0.35 µm technology.

4 STRUCTURE

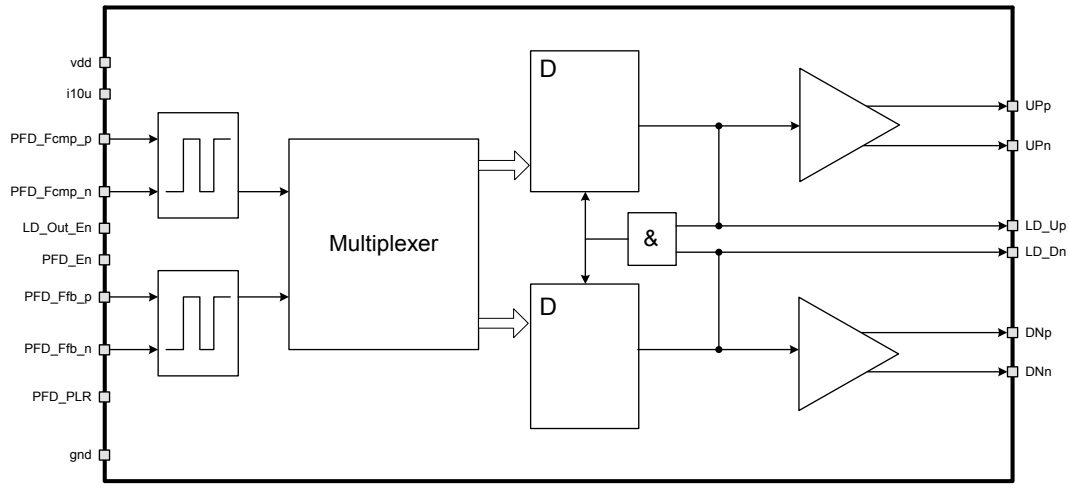

Figure 1: Phase-frequency detector in CMOS logic structure.

5 PIN DESCRIPTION

Name	Direction	Description
PFD_PLR	I	Input signal polarity
i10u	I	Reference current 10 µA
PFD_En	I	PFD enable/disable
PFD_Ffb_p	I	Differential input for divided VCO frequency signal
PFD_Ffb_n	I	
PFD_Fcmp_p	I	Differential input for reference frequency signal
PFD_Fcmp_n	I	
LD_Out_En	I	Enable/disable output signal for lock detector circuit
UPp	O	Output signal for increasing VCO control voltage
UPn	O	
DNp	O	Output signal for decreasing VCO control voltage
DNn	O	
LD_Up	O	Output signal for lock detector circuit
LD_Dn	O	
vdd	IO	Supply voltage
gnd	IO	Ground

6 LAYOUT DESCRIPTION

Phase-frequency detector dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	110	µm
Width	105	µm

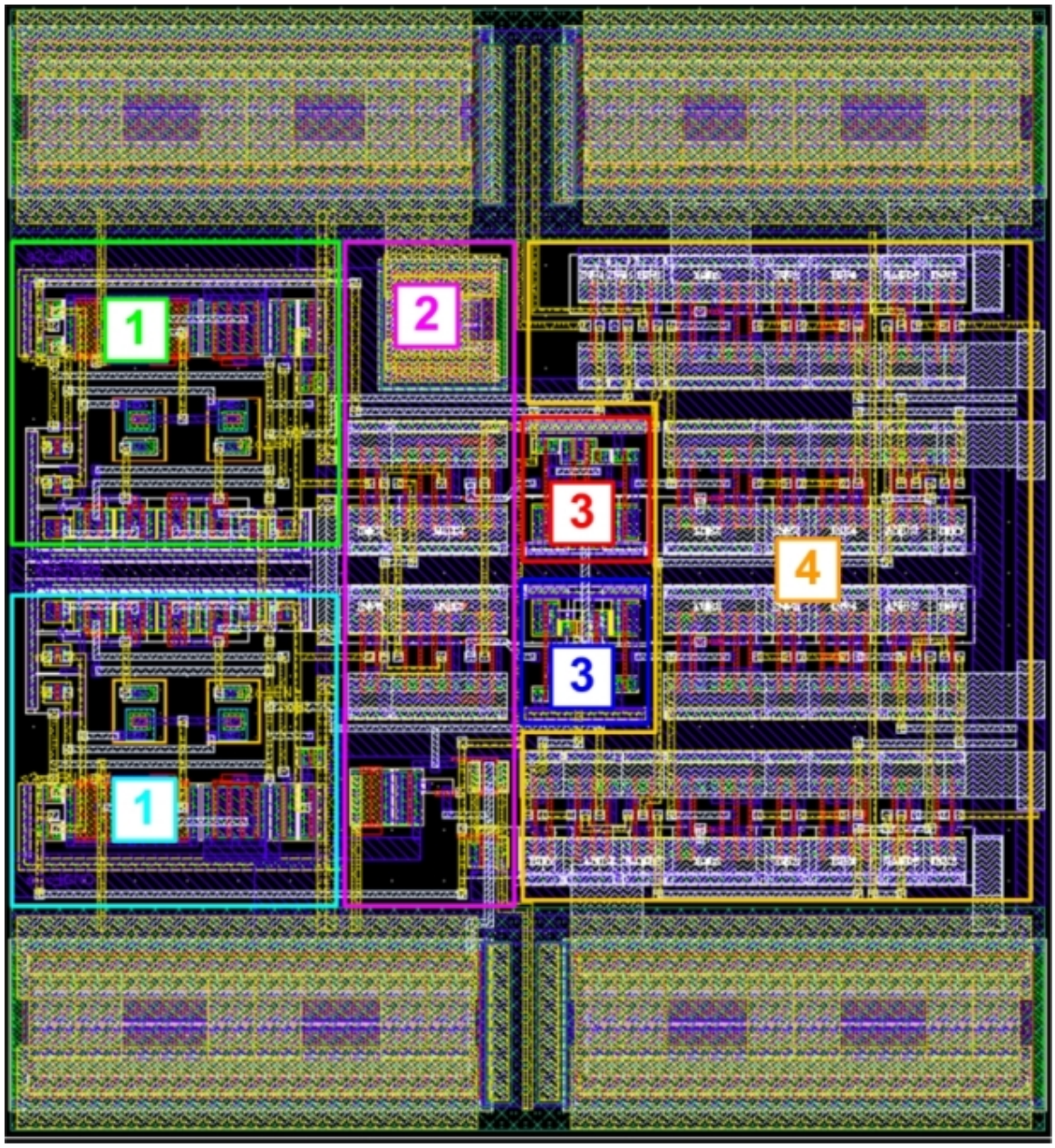

Figure 2: CMOS PFD structure.

1. ECL to CMOS signal converter
2. Multiplexer
3. D-flip-flop
4. Logic

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology AMS035 BiCMOS 0.35 µm
Status silicon proven
Area 0.012mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.5 ÷ 3.6 V, T = -40 ÷ +85 °C. Typical values are at V_{cc} = 2.7 V, T = +27° C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	2.5	2.7	3.6	V
Operating temperature range	T	-	-40	27	85	°C
Input signal frequency	F_{max}	-	-	-	100	MHz
Peak-to-peak input voltage	$A_{in\ p\text{-}p}$	At differential input	0.3	0.4	0.8	V
In-phase component signal input	$A_{in\ dc}$	V_{cc}=2.7 V	1.6	1.8	V_{cc} – 0.6	V
Reset delay	t_{rst}	-	0.9	1.9	3.3	ns
Current consumption	I_{dd}	V_{cc}=2.7 V	-	0.17	0.2	mA
Stand-by current	I_{st}	V_{cc}=2.7 V	-	-	10	nA
Input logic-level high	V_{IH}	For digital inputs	0.9 V_{cc}	-	V_{cc}	V
Input logic-level low	V_{IL}		-0.2	0	0.2	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

1. From version 1.0:
   - Section “Technical characteristics” (refer to page 4)