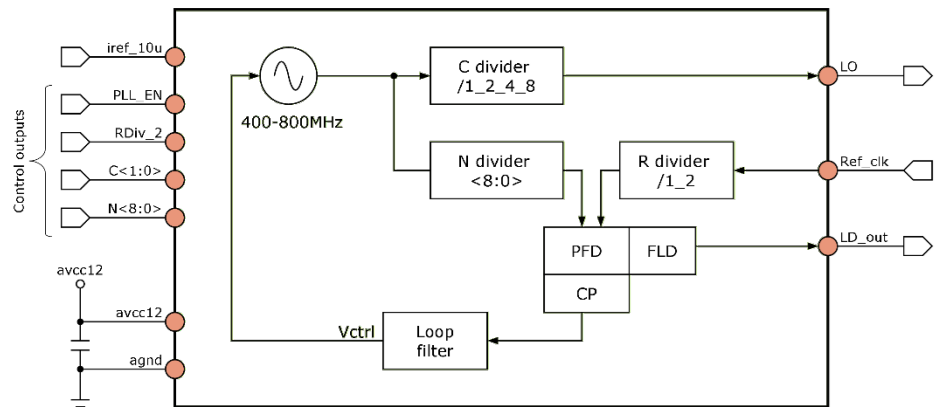


## 50-800MHz phase-locked loop frequency synthesizer

### OVERVIEW

055TSMC\_PLL\_01 is an integer-N phase-locked loop frequency synthesizer (PLL), which produces stable clock signal in range from 50 to 800MHz. It works with reference frequency from 4 to 20 MHz. The block includes 400-800MHz VCO, programmable N and R dividers, low noise digital



phase-frequency detector (PFD), charge pump (CP) with integrated loop filter, frequency lock detector (FLD) and programmable output clock C divider.

IP technology: TSMC CMOS 55nm.

IP status: silicon proven.

Area: 0.009 mm<sup>2</sup>.

### ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units		
			min	typ.	max			
Supply voltage	V <sub>avcc12</sub>	-	1.08	1.2	1.32	V		
Operating temperature range	T <sub>i</sub>	-	-45	25	+85	°C		
Reference current	I <sub>ref</sub>	-	-	10	-	μA		
Current consumption	I <sub>cc</sub>	F <sub>LO</sub> = 40MHz	-	200	300	μA		
		F <sub>LO</sub> = 800MHz	-	280	370			
Current consumption in standby mode	I <sub>stb</sub>	-	-	0.03	2.4	μA		
Input logic-level high	V <sub>IH</sub>	For digital inputs	V <sub>avcc12</sub> -0.25			V		
Input logic-level low	V <sub>IL</sub>		0	-	0.25	V		
Reference frequency range	F <sub>ref_clk</sub>	-	4	-	20	MHz		
Output frequency	F <sub>LO</sub>	-	50	200	800	MHz		
Phase noise	LO <sub>PN</sub>	F <sub>ref</sub> = 10MHz; F <sub>LO</sub> = 200MHz	@1MHz	-	-93.5	-	dBc/Hz	
			@10kHz	-	-103.6	-		
		F <sub>ref_clk</sub> = 6MHz	F <sub>LO</sub> = 200MHz	@100kHz	-	-101.7		-
			@1MHz	-	-102.2	-		
		F <sub>LO</sub> = 200MHz	@10kHz	-	-98.2	-		
			@1MHz	-	-92.9	-		
LO duty cycle	LO <sub>DC</sub>	-	40	50	60	%		
Ref clk duty cycle	Ref_clk <sub>DC</sub>	-	40	50	60	%		
LO RMS jitter value	J <sub>RMS</sub>	F <sub>ref</sub> = 10MHz; F <sub>LO</sub> = 200MHz; Ref_clk RMS jitter < 5ps; no other noisy devices on the synthesizer power supply	-	35	-	ps		
		F <sub>ref</sub> = 6MHz	F <sub>LO</sub> = 200MHz	-	28		-	
		F <sub>LO</sub> = 400MHz	-	21	-			
N dividing ratio	N	-	16	-	511	-		
C dividing ratio	C	-	1	-	8	-		
R dividing ratio	R	-	1	-	2	-		
Lock time	T <sub>lock</sub>	-	-	40	-	μs		
Lock detector accuracy	S <sub>err</sub>	-	-	5	-	ns		