Phase-locked loop clock generator

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- Low phase noise
- Low jitter
- Fully integrated 2GHz VCO
- Fully integrated loop filter with ability to use external loop filter
- Built-in lock detection circuit
- High reference frequency spur rejection
- Adjustable value of charge pump output current
- Built-in ADC for measuring VCO control voltage value
- Digital loop gain compensation
- Low current consumption
- Adjustable power supply voltage
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- Low jitter clock generation

3 OVERVIEW

It is a integer-N phase-locked loop frequency synthesizer (PLL) based on fully integrated 2GHz LC-VCO with low gain and fine phase noise performance. It work with reference frequency from 25 MHz XTAL oscillator or external signal source with frequency up to 500 MHz. Phase-frequency divider compare frequency can be equal or 2,3,4...63 times lower than reference. VCO frequency N-divider has programmable coefficient of division with step 1 in range 4 to 2047. Phase-frequency detector has built-in analog and digital lock detector circuits. Charge pump scheme with ADC and adjustable output current allow compensation VCO gain variation within band and keep loop gain constant. Integrated low-pass loop filter has adjustable values of resistance and capacitance for tune loop and get best phase-noise performance. All of output clocks have 0.5 duty cycle value using duty cycle recovery circuit.

4 STRUCTURE

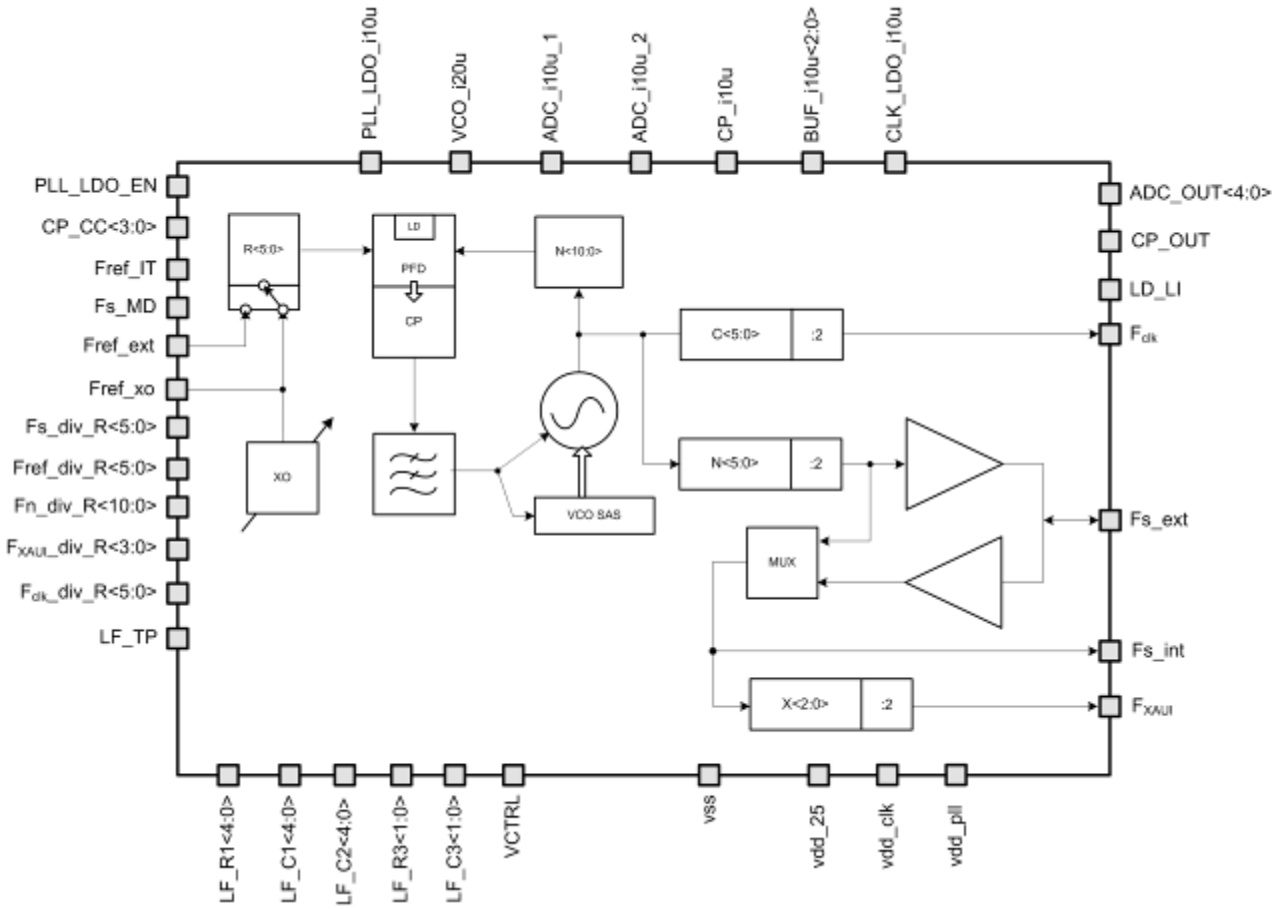

Figure 1: Phase-locked loop clock generator structure.

5 PIN DESCRIPTION

Name	Direction	Description
PLL_LDO_i10u	I	LDO voltage regulator reference current 10 uA
VCO_i20u	I	VCO reference current 20 uA
ADC_i10u_1	I	ADC reference current 10 uA line 1
ADC_i10u_2	I	ADC reference current 10 uA line 2
CP_i10u	I	Charge pump reference current 10 uA
BUF_i10u<2:0>	I	Reference currents 3x10 uA for duty cycle correction circuits
CLK_LDO_i10u	I	LDO voltage regulator reference current 10 uA
PLL_LDO_En	I	Enable/Disable of PLL low drop-out voltage regulator
CP_CC<3:0>	I	Charge pump output current adjustment
F_{ref}_IT	I	External reference frequency type
Fs_MD<1:0>	I	Sampling frequency management
Fref_ext	I	External reference frequency input
Fref_xo	I	Internal reference frequency input
s_div_R<5:0>	I	FVCO/FS frequency ratio (2-126)
Fref_div_R<5:0>	I	Reference frequency division ratio (1-63)
Fn_div_R<10:0>	I	Reference frequency division ratio (4-2047)
Fxaui_div_R<3:0>	I	FVCO/FXAUI frequency ratio (1-14)
Fclk_div_R<5:0>	I	FVCO/FCLK frequency ratio (2-126)
LF_TP	I	PLL loop filter type
LF_R1<4:0>	I	PLL loop filter resistance R1 value adjustment
LF_C1<4:0>	I	PLL loop filter capacitance C1 value adjustment
LF_C2<4:0>	I	PLL loop filter capacitance C2 value adjustment
LF_R3<1:0>	I	PLL loop filter resistance R3 value adjustment
LF_C3<1:0>	I	PLL loop filter capacitance C3 value adjustment
VCTRL	I	VCO control voltage from external loop filter
ADC_OUT<4:0>	O	PLL Analog-to-digital converter output (digital value of VCO control voltage) Code interpretation
CP_OUT	O	Charge pump output for external loop filter circuit
LD_LI	O	Lock indicator
Fclk	O	CLK frequency output
Fs_ext	IO	Sampling frequency input/output node
Fxaui	O	XAUI frequency output
Fs_int	O	Sampling frequency output for internal circuits

Table “Pin description” (continue)

Name	Direction	Description
vss	IO	Ground
vdd_25	IO	External 2.5V power supply line
vdd_pll	IO	PLL power supply line (LDO voltage regulator output)
vdd_clk	IO	CLK power supply line (LDO voltage regulator output)

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	880	µm
Width	1080	µm

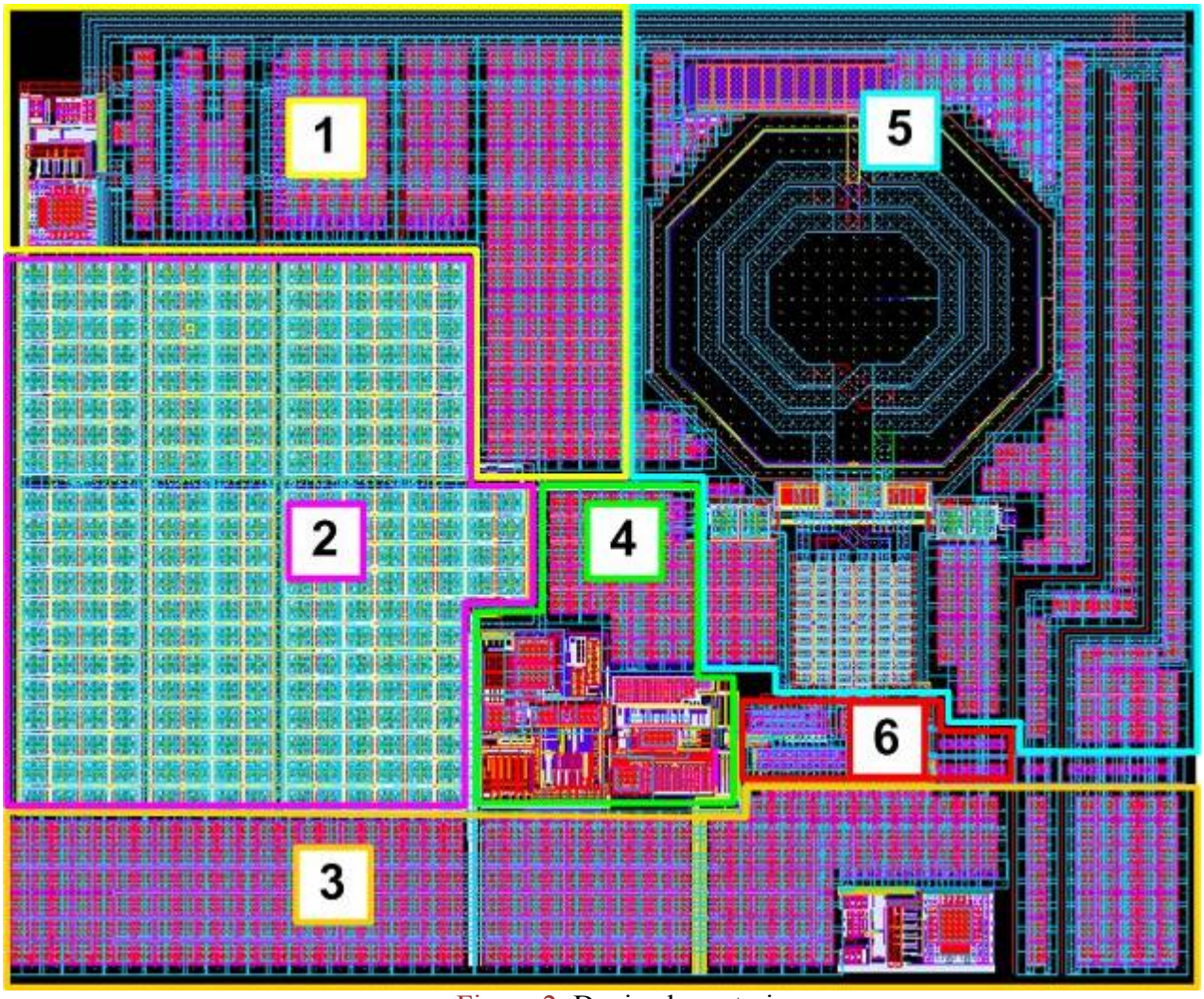

Figure 2: Device layout view.

1. PLL LDO voltage regulator
2. Loop filter
3. CLK LDO voltage regulator
4. Phase-frequency detector with Charge pump
5. VCO
6. Frequency dividers

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS CRN65LP
Status silicon proven
Area 0.95 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd_25} = 2.375 ÷ 2.625 V and T = -40 ÷ +125°C. Typical values are at V_{dd_25} = 2.5 V, T = +85 °C, unless otherwise specified.

Parameter	Symbol	Condition		Value			Unit
				min	typ	max	
Supply voltage	V_{dd_25}	-		2.375	2.5	2.625	V
VCO control voltage	V_{ctrl}	-		0.5	-	2.0	V
Internal regulated supply voltage	V_{dd_pll}	From bandgap reference:					V
		LDO preset=1.16V		1.144	1.164	1.182	
		LDO preset=1.20V		1.181	1.200	1.217	
		LDO preset=1.24V		1.221	1.241	1.257	
		LDO preset=1.28V		1.258	1.277	1.293	
Temperature range	T	-		-40	85	125	°C
VCO frequency range	F_{vco}	Typical case		1850	-	2140	MHz
Internal reference frequency	F_{ref_int}	-		-	25	-	MHz
External reference frequency	F_{ref_ext}	-		25	-	500	MHz
Phase-detector frequency	F_{pfd}	-		-	-	250	MHz
Phase noise	N	F_s = 500MHz	Frequency offset:				dB/Hz
			10kHz	-	-97	-	
			100kHz	-	-99	-	
			1MHz	-	-124	-	
			10MHz	-	-135	-	
Period jitter (rms)	J	F_s = 500MHz		-	2.12	-	ps
Charge pump sink/source current value mismatch	I_{cp_mis}	0.5 V < V_{ctrl} < 2 V		-	-	4	%
Charge pump sink and source current matching	I_{cp_m}	0.5 V < V_{ctrl} < 2 V		-	-	3	%
Charge pump sink/source current value	I_{cp}	-		20	-	320	uA
Internal loop filter R1 value	R1	-		5	-	82.5	kOhm
Internal loop filter C1 value	C1	-		24	-	768	pF
Internal loop filter C2 value	C2	-		3	-	96	pF
Fs frequency value	F_S	Full voltage swing 45..55% duty cycle		107	-	750	MHz
Fxaui frequency value	F_{XAUI}	Full swing voltage 45..55% duty cycle		50	-	750	MHz
Fclk frequency value	F_{clk}	Reduced voltage swing 45..55% duty cycle		12	-	750	MHz
Reference frequeny divider ratio	R_{div}	-		1	-	31	
VCO frequency divider ratio	N_{div}	-		4	-	2047	
Standby current	I_{st}	Without input signal			<1		uA
Current consumption with buffer	Ibuf	-		-	30	-	mA

Table “Electrical characteristics” (continue)

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Input logic-high level	V_{IH}	-	$0.8V_{dd\_25}$		V_{dd_25}	V
Input logic-low level	V_{IL}	-	0	-	0.2	V

8 TYPICAL CHARACTERISTICS

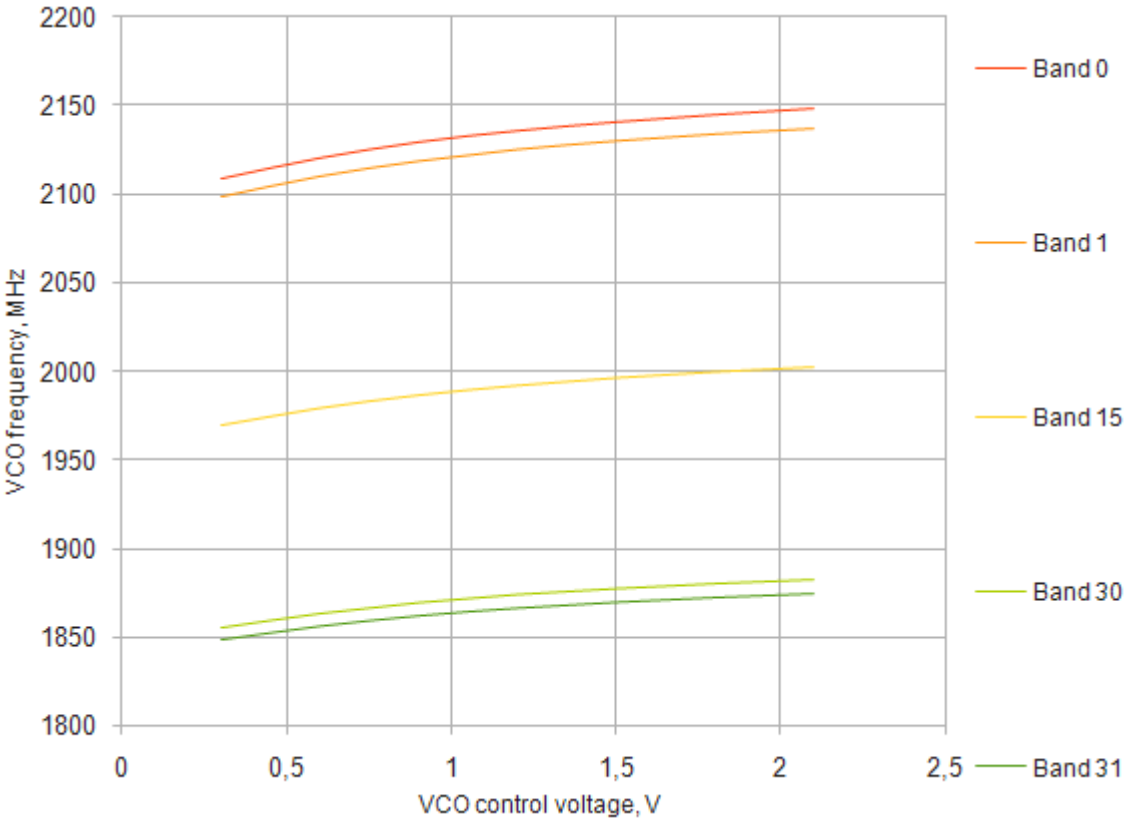

Figure 3: Simulated VCO tuning curves.

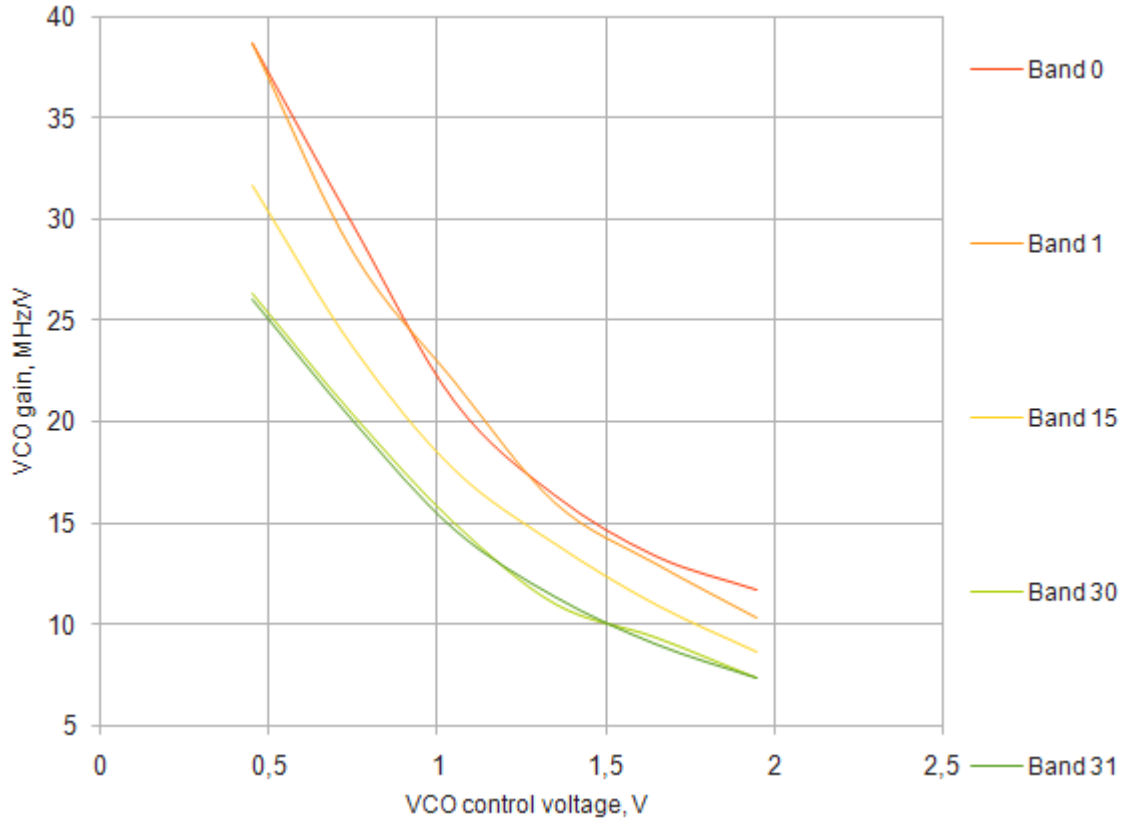

Figure 4: Simulated VCO gain.

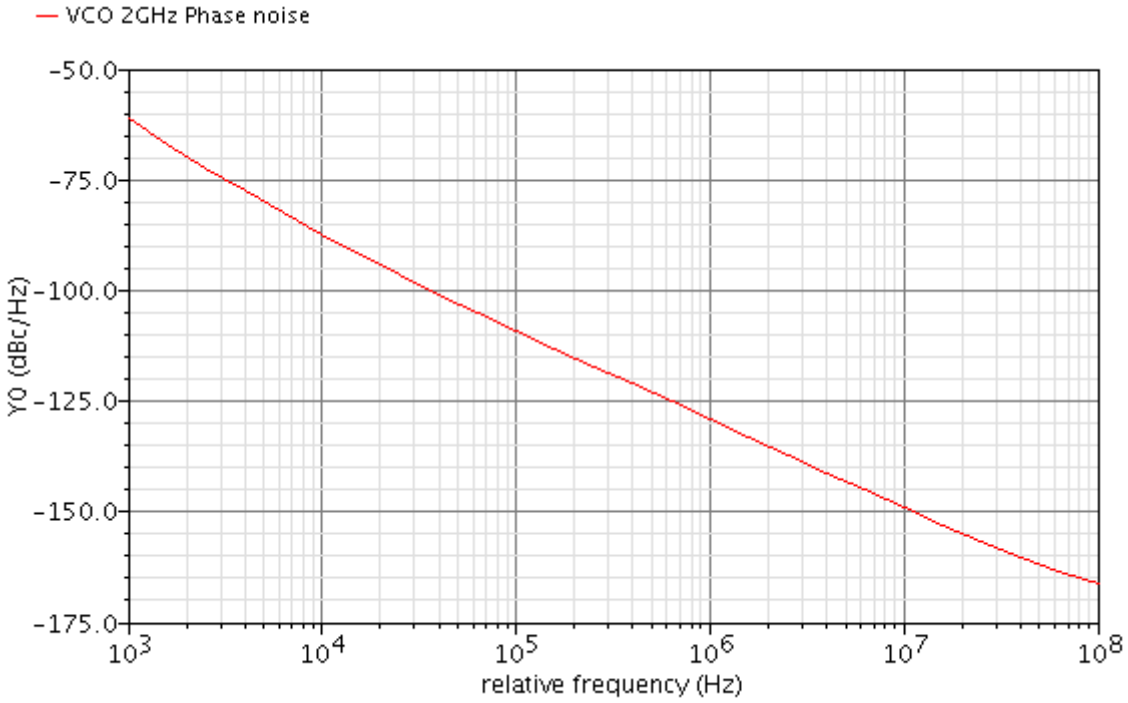

Figure 5: Simulated VCO open loop phase noise.

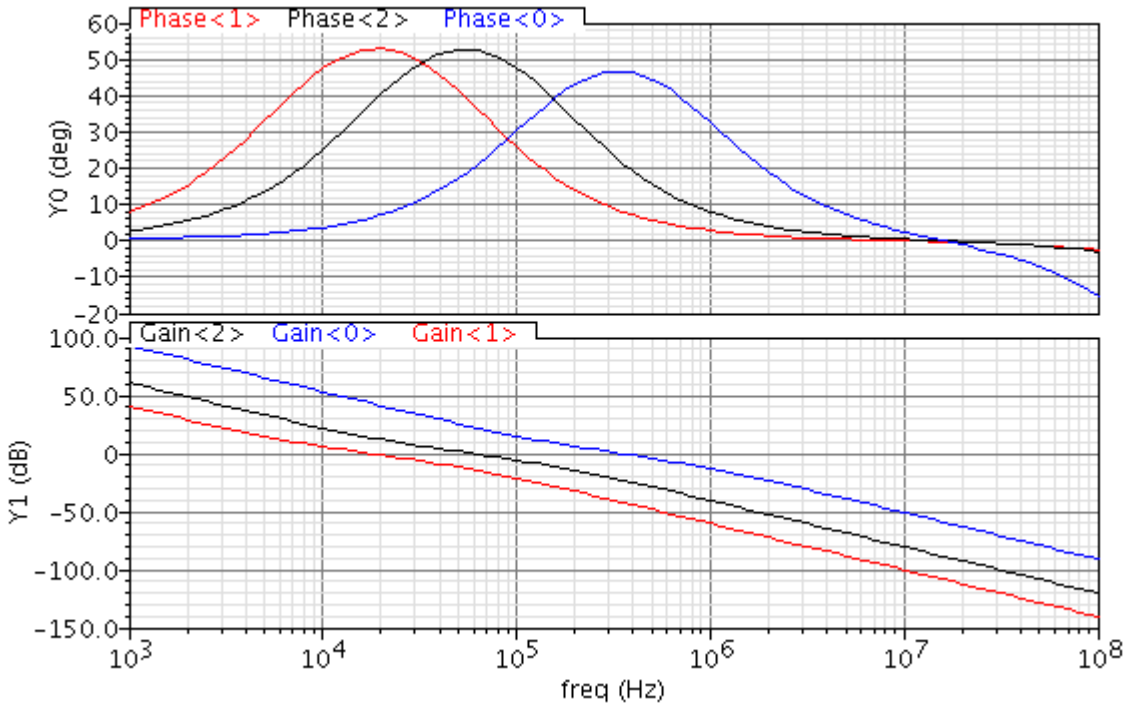

Figure 6: PLL open loop gain with minimum/center/maximum internal loop filter cutoff settings.

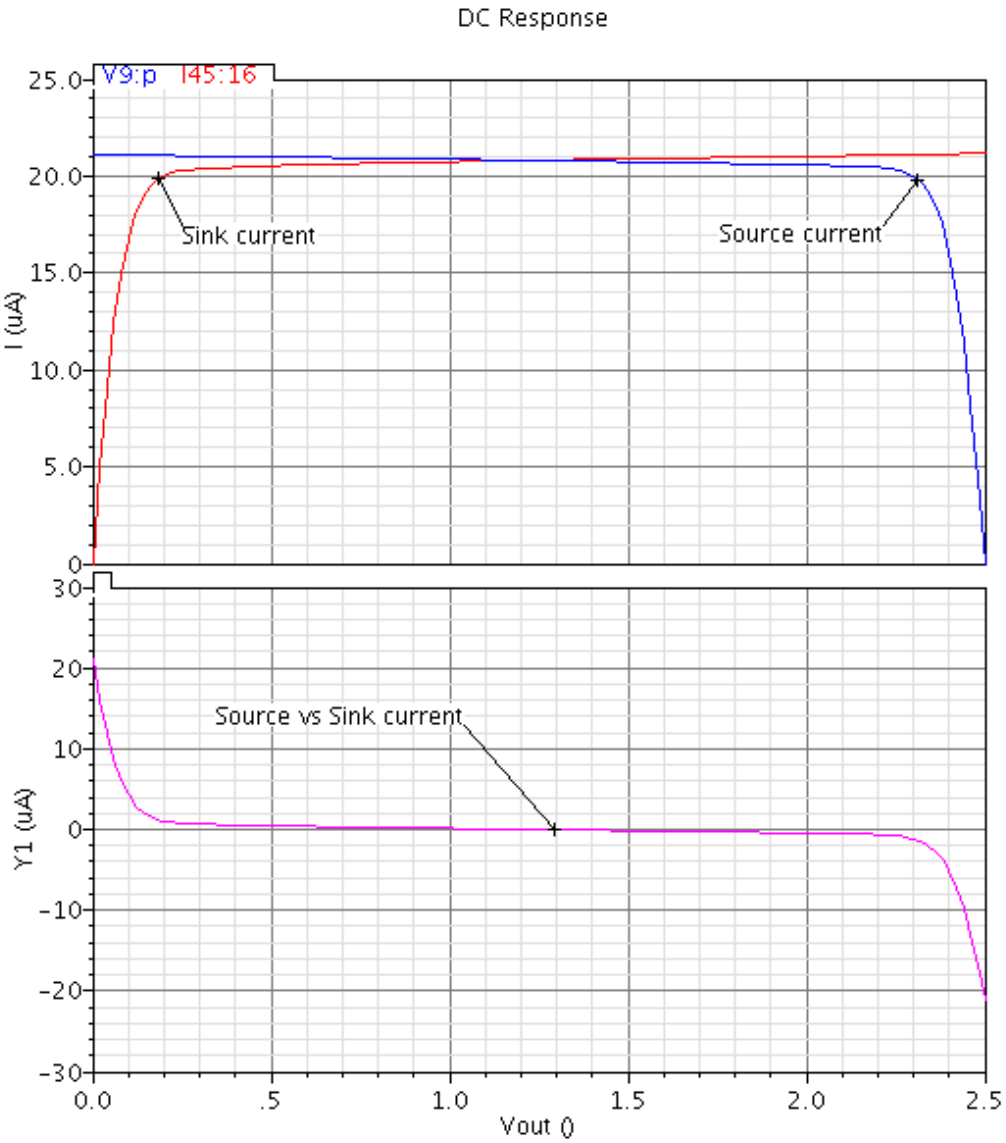

Figure 7: Charge pump output current (min current preset).

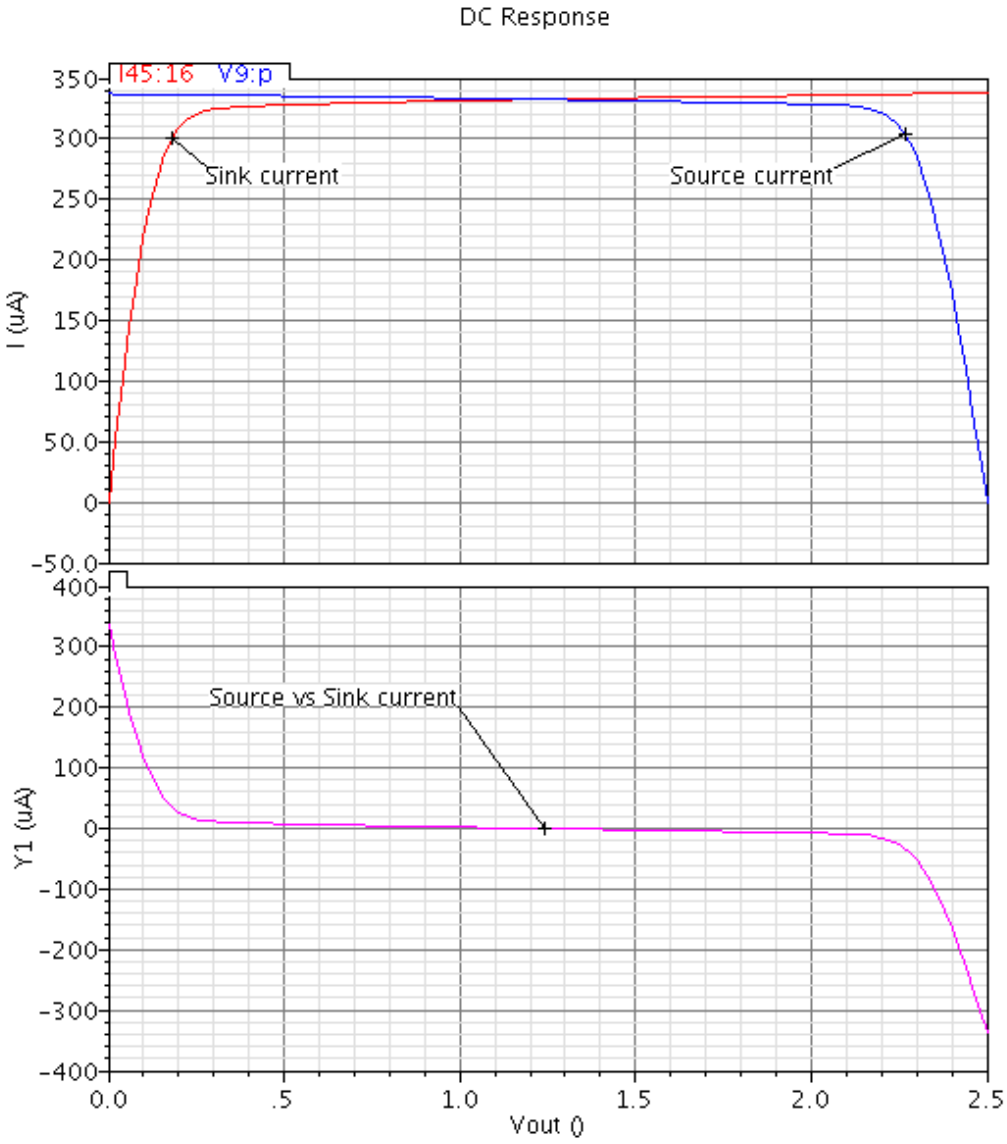

Figure 8: Charge pump output current (max current preset).

9 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation