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## Wide band 3GHz-6GHz phase-locked loop

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### SPECIFICATION

#### 1 FEATURES

- TSMC CMOS 65 nm
- Integer-N phase-locked loop
- Wide frequency range from 3GHz to 6GHz.
- Good phase noise performance
- Fully integrated VCO
- Fully integrated loop filter with ability to use external loop filter
- Built-in lock detection circuit
- High reference frequency spurious rejection
- Adjustable value of charge pump output current
- Built-in ADC for measuring VCO control voltage value
- Digital loop gain compensation
- Low current consumption
- Adjustable power supply voltage
- Portable to other technologies (upon request)

#### 2 APPLICATION

- RF receivers, transmitters, transceivers
- High frequency clock generation

#### 3 OVERVIEW

It is a integer-N phase-locked loop frequency synthesizer(PLL) based on fully integrated wide band LC-VCO with range from 3GHz to 6GHz with good phase noise performance. It work with reference frequency from 25MHz XTAL oscillator or external signal source with frequency up to 500 MHz. Phase-frequency divider compare frequency can be equal or 2,3,4...63 times lower than reference. VCO frequency N-divider has programmable coefficient of division with step 1 in range 4 to 2047. Phase-frequency detector has built-in analog and digital lock detector circuits. Charge pump scheme with ADC and adjustable output current allow compensation VCO gain variation within band and keep loop gain constant. Integrated low-pass loop filter has adjustable values of resistance and capacitance for tune loop and get best phase-noise performance.

## 4 STRUCTURE

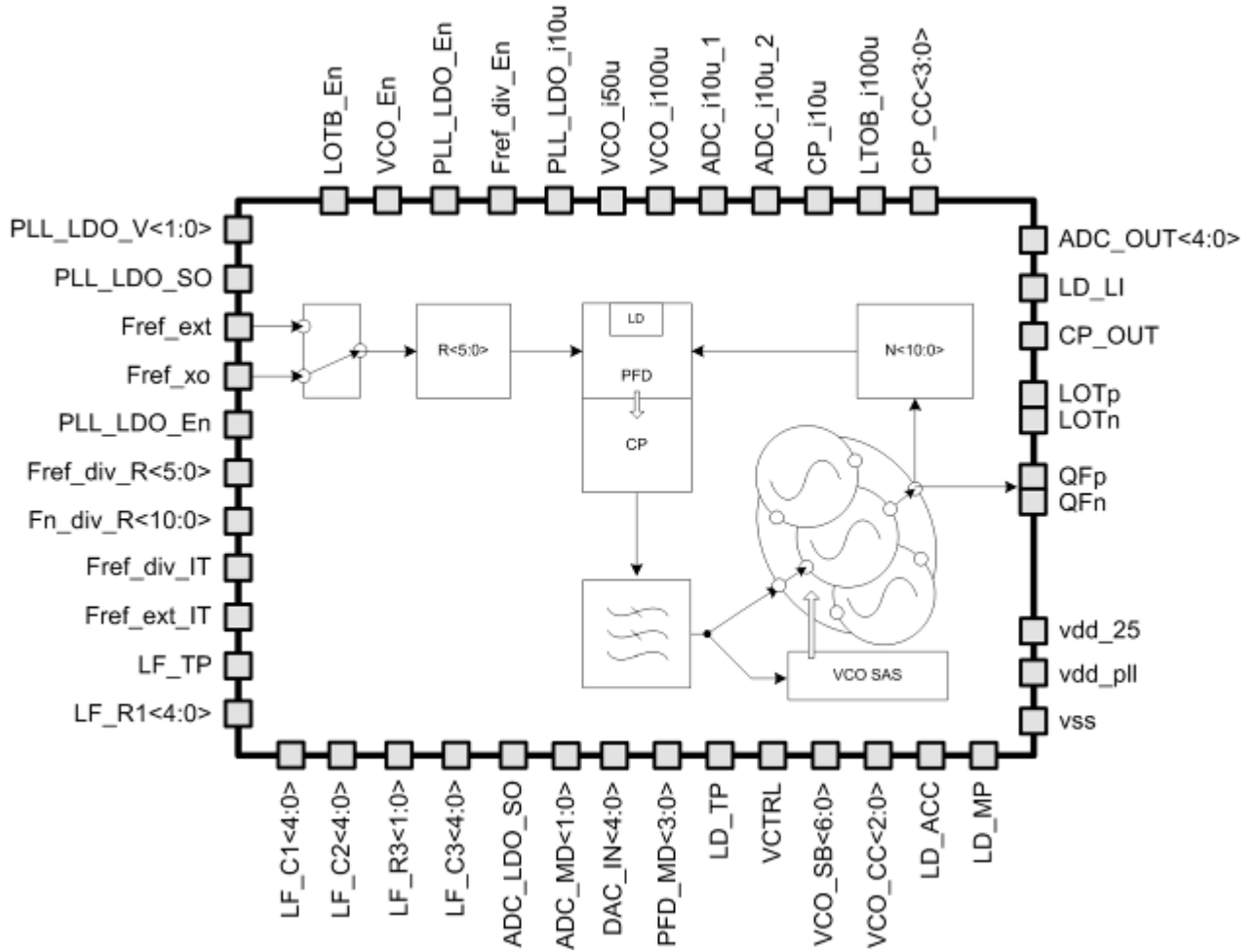


Figure 1: Wide band 3GHz-6GHz phase-locked loop structure

## 5 PIN DESCRIPTION

Name	Direction	Description
PLL_LDO_i10u	I	LDO voltage regulator reference current 10 uA
VCO_i50u	I	VCO reference current 50 uA
VCO_i100u	I	VCO buffer reference current 100 uA
ADC_i10u_1	I	ADC reference current 10 uA line 1
ADC_i10u_2	I	ADC reference current 10 uA line 2
CP_i10u	I	Charge pump reference current 10 uA
LOTB_i100u	I	LO test buffer reference current 100 uA
LOTB_En	I	Enable/Disable of LO test buffer
VCO_En	I	Enable/Disable of PLL voltage controlled oscillator
PLL_LDO_En	I	Enable/Disable of PLL low drop-out voltage regulator.
Fref_div_En	I	Enable/Disable of PLL reference frequency divider
PLL_LDO_V<1:0>	I	PLL power supply voltage adjustment
PLL_LDO_SO	I	Short out PLL power supply voltage to 2.5V line.
Fref_div_R<5:0>	I	Reference frequency division ratio (1-63)
Fn_div_R<10:0>	I	Reference frequency division ratio (4-2047)
Fref_div_IT	I	Reference frequency divider Input signal selection
Fref_ext	I	External reference frequency input
Fref_ext_IT	I	External reference frequency input signal type
Fref_xo	I	XTAL reference frequency input
VCO_CC<2:0>	I	VCO current control (4.0 mA — 9.6 mA)
VCO_SB<6:0>	I	VCO sub-band selection
VCTRL	I	VCO control voltage from external loop filter
LF_TP	I	PLL loop filter type
LF_R1<4:0>	I	PLL loop filter resistance R1 value adjustment
LF_C1<4:0>	I	PLL loop filter capacitance C1 value adjustment
LF_C2<4:0>	I	PLL loop filter capacitance C2 value adjustment
LF_R3<1:0>	I	PLL loop filter resistance R3 value adjustment
LF_C3<4:0>	I	PLL loop filter capacitance C3 value adjustment
ADC_LDO_SO	I	Short out DAC power supply voltage to 2.5V line
ADC_MD<1:0>	I	Analog-to-digital converter mode setup

Table “Pin description” (continue).

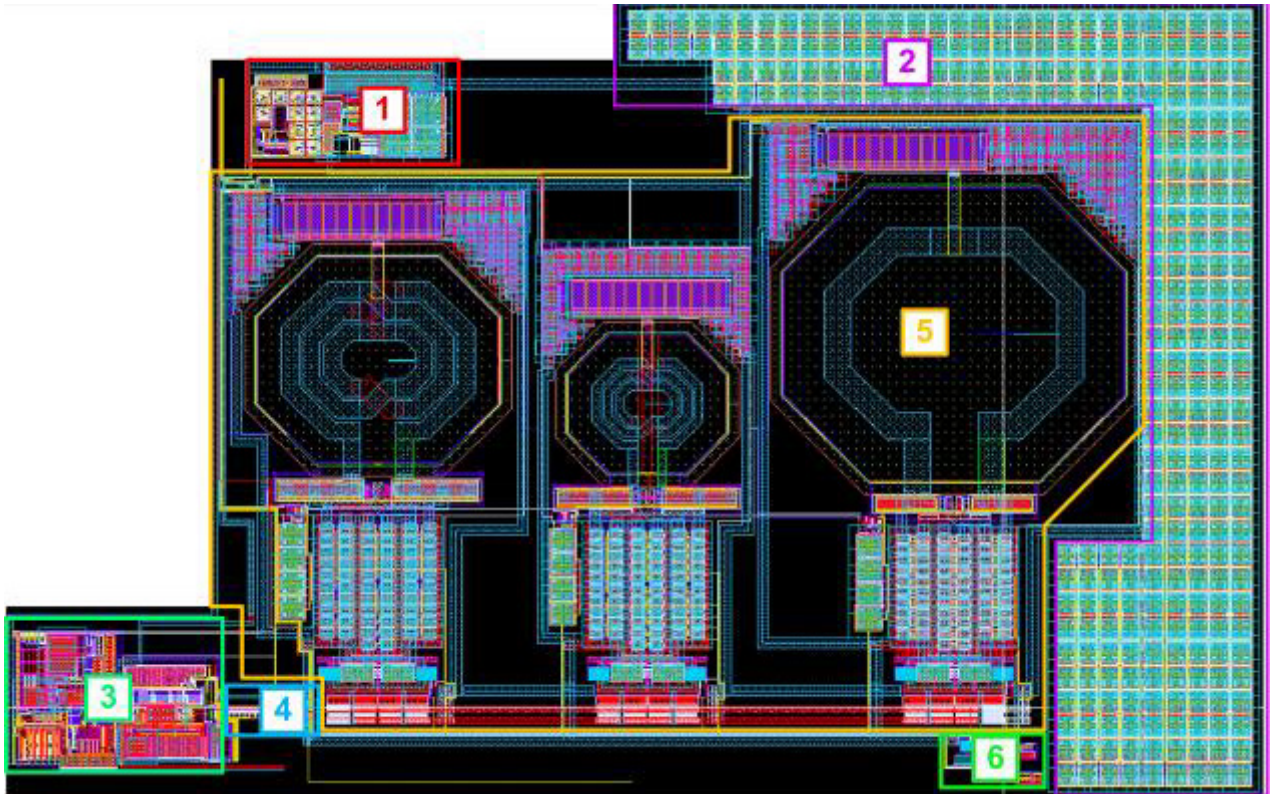
Name	Direction	Description
DAC_IN<4:0>	I	If VCO test mode enabled (ADC_MD<1:0> = “11”) set VCO control voltage
		else set ADC clock frequency
PFD_MD<3>	I	Phase-frequency detector polarity
PFD_MD<2>	I	Lock detector circuit control
PFD_MD<1:0>	I	Phase-frequency detector with charge pump and lock detector circuits mode setup
LD_TP	I	Lock detector circuit.
LD_ACC	I	Lock detection accuracy(for analog circuit).
LD_MP	I	Lock detection refresh time(for analog circuit).
CP_CC<3:0>	I	Charge pump output current adjustment
ADC_OUT<4:0>	O	PLL Analog-to-digital converter output (digital value of VCO control voltage)
LD_LI	O	Lock indicator
CP_OUT	O	Charge pump output for external loop filter circuit
LOTp	O	LO test signal nodes
LOTn	O	
QFp	O	VCO output nodes
QFn	O	
vdd_25	IO	External 2.5V power supply line
vdd_pll	IO	PLL power supply line (LDO voltage regulator output)
vss	IO	Ground

## 6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

**Table 1:** Block dimensions.

Dimension	Value	Unit
Height	900	$\mu\text{m}$
Width	1420	$\mu\text{m}$



**Figure 2:** Device layout view

1. PLL LDO voltage regulator
2. Loop filter
3. Phase-frequency detector with Charge pump
4. Dividers
5. VCO
6. Output buffer

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ TSMC CMOS CRN65LP  
 Status \_\_\_\_\_ silicon proven  
 Area \_\_\_\_\_ 1.08 mm<sup>2</sup>

### 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{cc25} = 2.375 \div 2.625$  V and  $T = -40 \div 125^{\circ}\text{C}$ . Typical values are at  $V_{cc}=2.5$  V,  $T=+85^{\circ}\text{C}$ , unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	$V_{cc25}$	-	2.375	2.5	2.625	V
Operating temperature range	T	-	-40	+85	+125	$^{\circ}\text{C}$
VCO control voltage	$V_{ctrl}$	-	0.5	-	2.0	V
Internal regulated supply voltage	$V_{dd\_pll}$	From bandgap reference				V
		LDO preset=1.16V	1.144	1.164	1.182	
		LDO preset=1.20V	1.181	1.200	1.217	
		LDO preset=1.24V	1.221	1.241	1.257	
		LDO preset=1.28V	1.258	1.277	1.293	
VCO frequency range	$F_{vco}$	Typical case	2790	-	6270	MHz
VCO minimum frequency	$F_{vcomin}$	Guaranteed	-	-	2890	MHz
VCO maximum frequency	$F_{vcomax}$	Guaranteed	6080	-	-	MHz
VCO gain	$K_{vco}$	-	25	90	230	MHz/V
Open loop VCO phase noise performance	$PN_{VCO}$	Frequency offset:				dBc/Hz
		10 kHz	-65	-71	-78	
		100 kHz	-89	-94	-100	
		1 MHz	-109	-115	-121	
		10 MHz	-129	-135	-141	
VCO buffer output amplitude	$V_{p-p}$	-	0.8	1.1	-	V
Internal reference frequency	$F_{ref\_int}$	-	-	25	-	MHz
External reference frequency	$F_{ref\_ext}$	-	25	-	500	MHz
Phase-detector frequency	$F_{pfd}$	-	-	-	250	MHz
Charge pump sink/source current value mismatch	$I_{cp\_mis}$	$0.5\text{ V} < V_{ctrl} < 2\text{ V}$	-	4	5	%
Charge pump sink vs. source current matching	$I_{cp\_m}$	$0.5\text{ V} < V_{ctrl} < 2\text{ V}$	-	2.5	3	%
Charge pump sink/source current value	$I_{cp}$	(adjustable)	20	-	320	$\mu\text{A}$
Internal loop filter cut off frequency available settings	$LF_{cf}$	Charge pump settings:				kHz
		20 $\mu\text{A}$	30	-	125	
		120 $\mu\text{A}$	75	-	350	
		320 $\mu\text{A}$	125	-	500	
Internal loop filter R1 value	R1	(adjustable)	5	-	82.5	kOhm
Internal loop filter C1 value	C1	(adjustable)	24	-	768	pF
Internal loop filter C2 value	C2	(adjustable)	3	-	96	pF
Reference frequency spurious suppression	$SS_{rf}$	-	-	70	-	dB
Reference frequency divider ratio	Rdiv	-	1	-	31	-
VCO frequency divider ratio	Ndiv	-	4	-	2047	-
Standby current	$I_{sb}$	Without input signal	-	<1	-	$\mu\text{A}$
Current consumption	$I_{dc}$	Default config DC	-	9.5	-	mA
Input logic-high level	$V_{HL}$	-	$0.85V_{dd}$	-	$1.15V_{dd}$	V
Input logic-low level	$V_{IL}$	-	-0.2	-	+0.2	V

## 8 TYPICAL CHARACTERISTICS

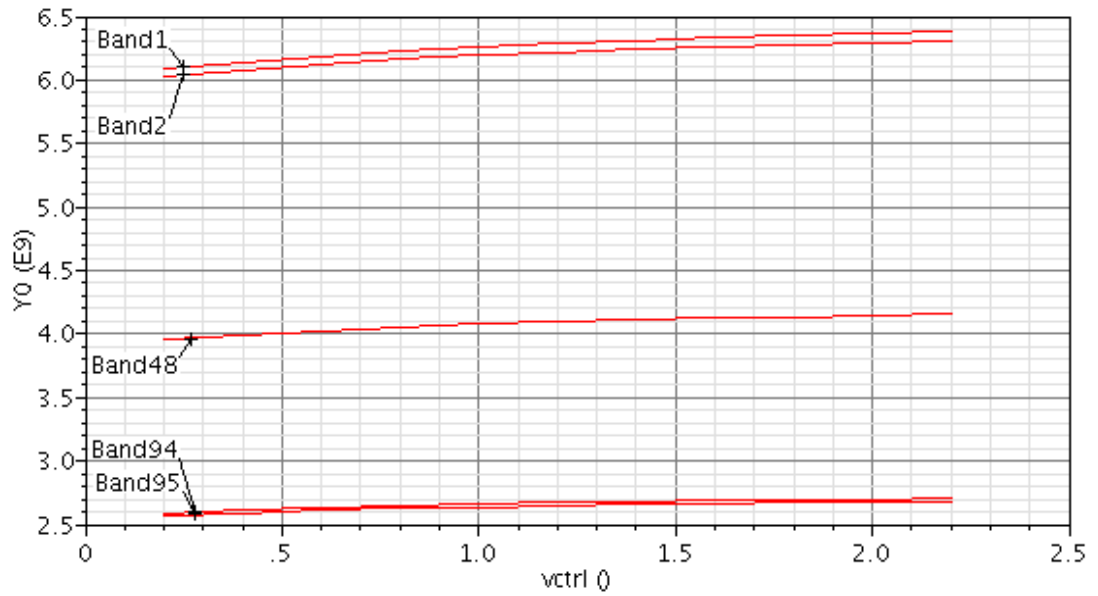


Figure 3: Simulated VCO tuning curves

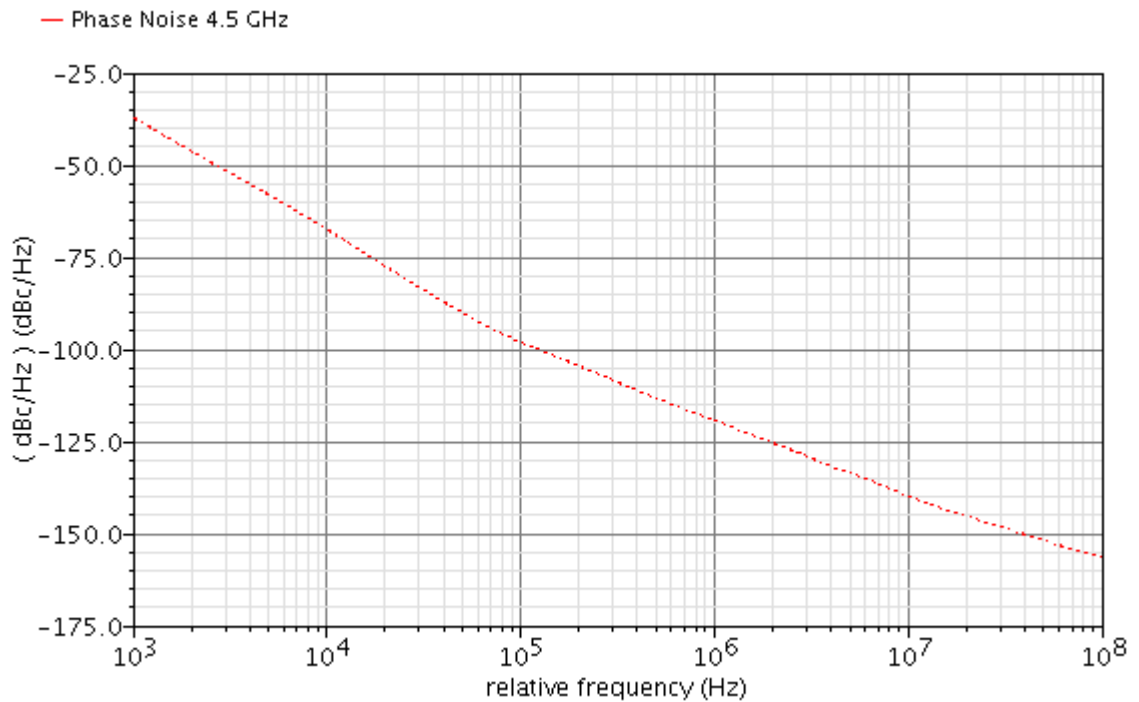


Figure 4: Simulated VCO open loop phase noise

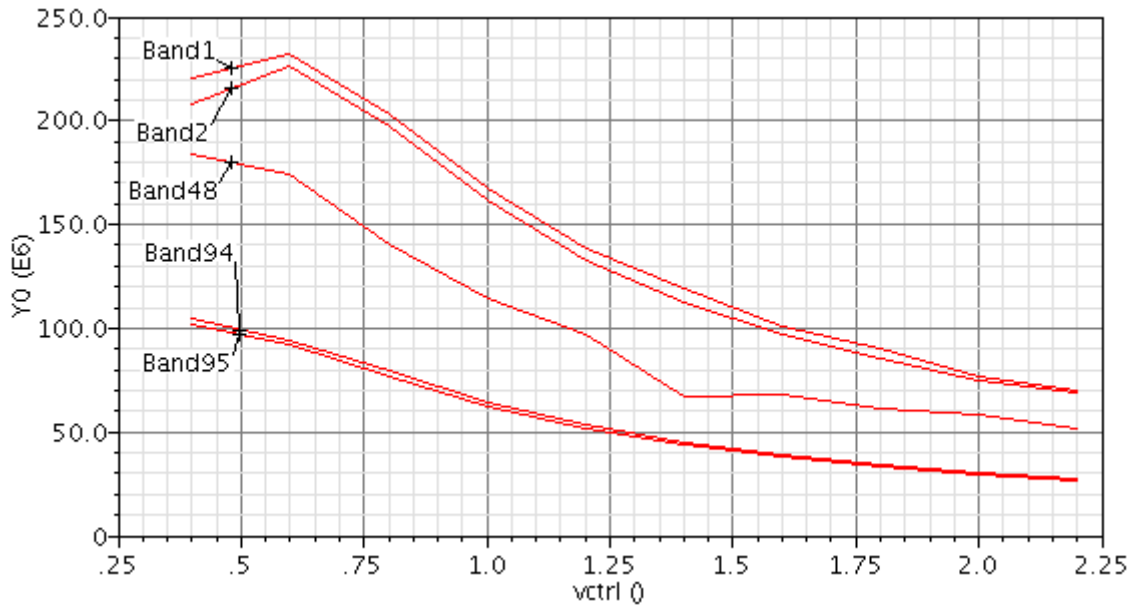


Figure 5: Simulated VCO gain

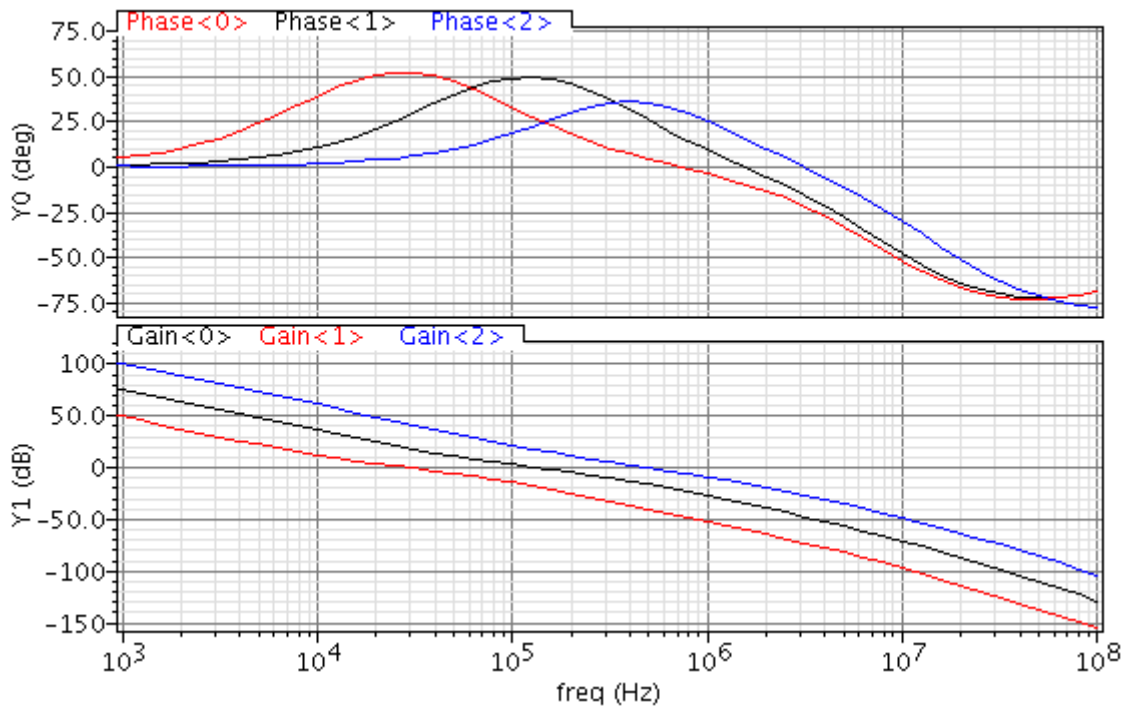
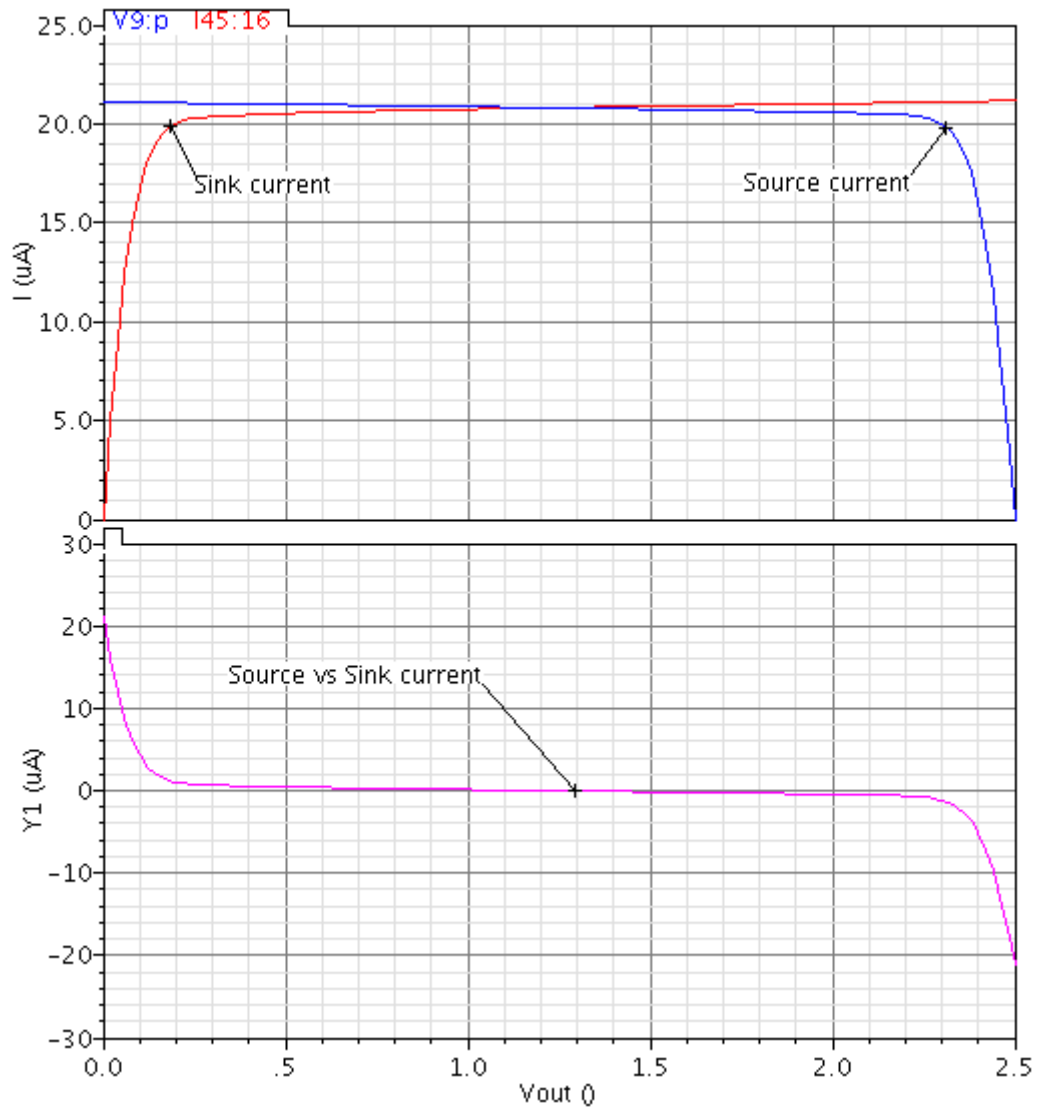


Figure 6: PLL open loop gain with minimum/center/maximum internal loop filter cutoff settings





**Figure 7:** Charge pump output current (min current preset)

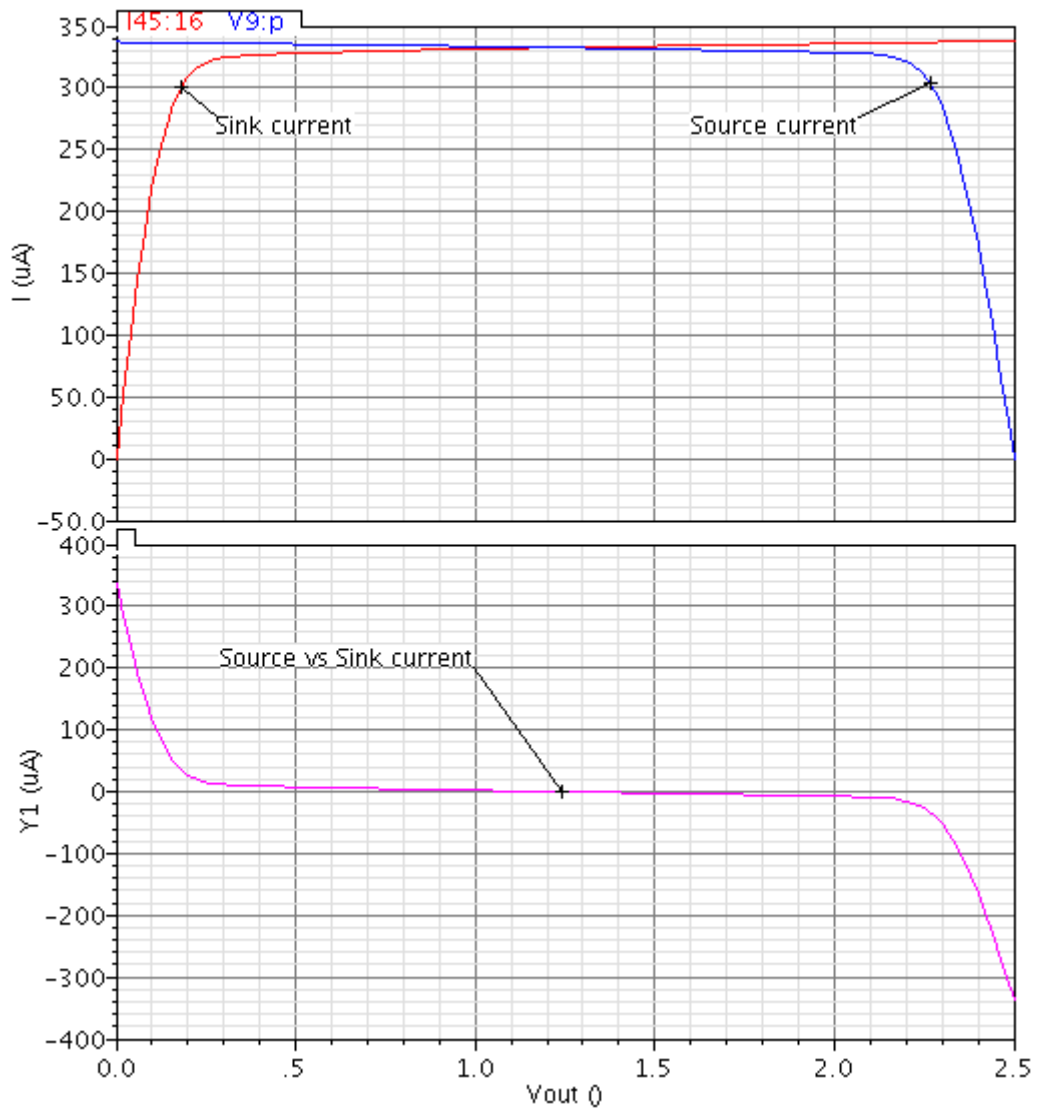


Figure 8: Charge pump output current (max current preset)

## 9 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation