50 – 800 MHz phase-locked loop

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- Output frequency from 50 to 800 MHz
- Reference frequency from 4 to 30 MHz
- Power supply 1.2 V
- CMOS output
- Supported foundries: TSMC, UMC, Global Foundries

2 APPLICATION

- Digital circuit clocking

3 OVERVIEW

The synthesizer forms clock signal with frequency from 50 to 800 MHz. It consists of the ring VCO with frequency from 400 to 800 MHz, a programmable feedback divider, a low noise digital phase noise detector (PFD), a precision charge pump (CP) with internal loop filter, lock detector (LD) and programmable clock divider to obtain a required output frequency.Output frequency is calculated by formula: $F_{LO} = (F_{ref}*N)/(R*C)$. Output signal is CMOS compatible.

4 STRUCTURE

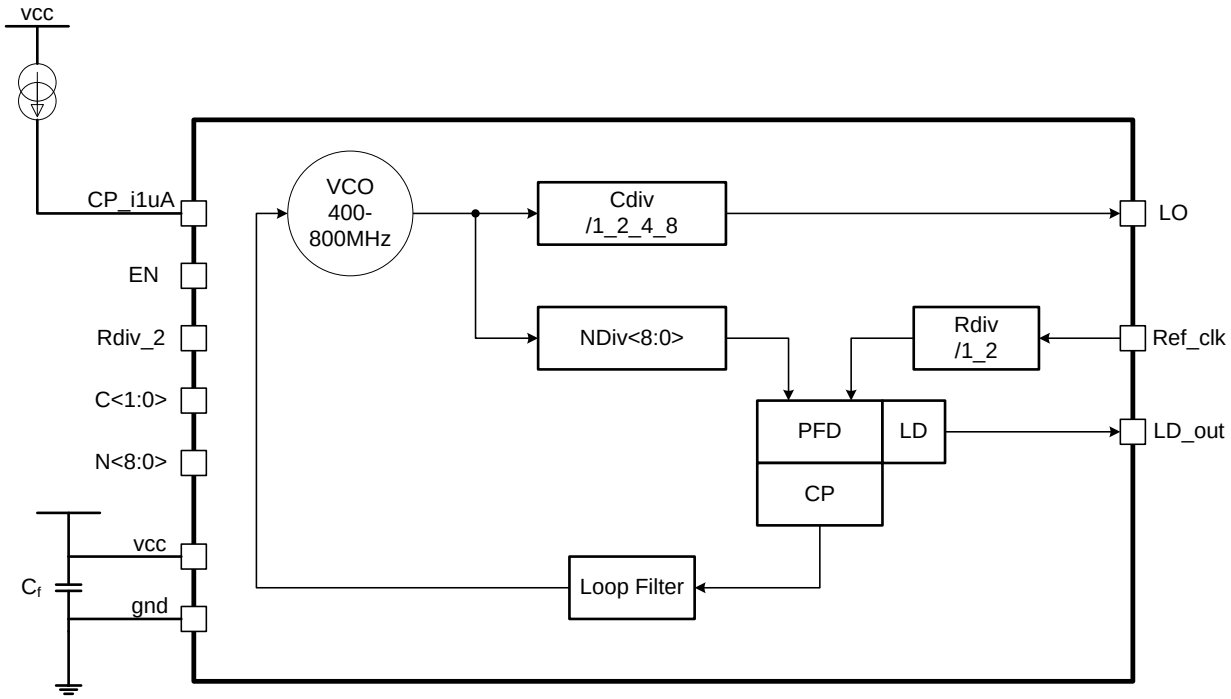

Figure 1: PLL structure

5 PIN DESCRIPTION

Name	Direction	Description
CP_i1uA	I	Reference current for CP 0.85 uA (source from power)
EN	I	Block enable/ disable: “0” disable “1” enable
Ref_clk	I	Reference frequency oscillator signal (1.2 V)
Rdiv_2	I	Set R dividing ratio: “0” 1 “1” 2
C<1:0>	I	C divider integer ratio: “00” 1 “01” 2 “10” 4 “11” 8
N<8:0>	I	N divider integer ratio (16-511)
LO	O	Output frequency signal. $F_{LO} = (F_{ref}*N)/(R*C)$
LD_out	O	Lock detector signal
vcc	P	Power supply 1.2 V
gnd	P	Ground

Notes: I – input, O – output, P – power

6 LAYOUT DESRIPTION

6.1 TECHNOLOGY OPTIONS

PLL is designed under TSMC 65nm LP (CLN65LP) technology process with following options and elements:

- 4 metal levels are used for routing
- 1.2V standard VT NMOS and PMOS transistors
- 1.2V NATIVE NMOS transistor
- P+ poly resistor without salicide
- 2.5V Standard-Vt NMOS in N-Well varactor

6.2 PHYSICAL DIMENSIONS

The block PLL dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	125	um
Width	70	um

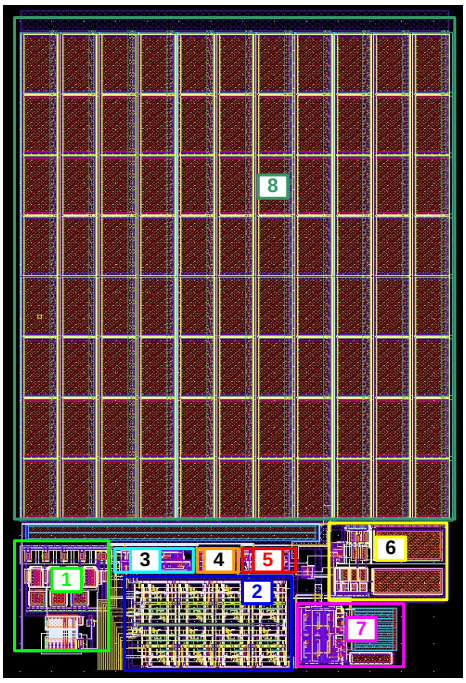

Figure 2: PLL layout

1. VCO
2. NDivider
3. CDivider
4. RDivider
5. PFD
6. Charge Pump
7. Lock detector
8. Loop filter

6.3 THIRD PARTIES IP

065TSMC_PLL_10 utilizes instances from standard logic cells library: tcbn65lp.

7 INTEGRATION GUIDELINES

7.1 INPUT AND OUTPUT SIGNALS

Input and output signals have intrinsic capacitance up to 20 fF.
Input signals must have rising/falling edges no more than 0.5 ns, excepting Ref_clk that must have rising/falling edges no more than 0.15ns. Transitions are measured at levels 0.1*VCC and 0.9*VCC (see Figure).

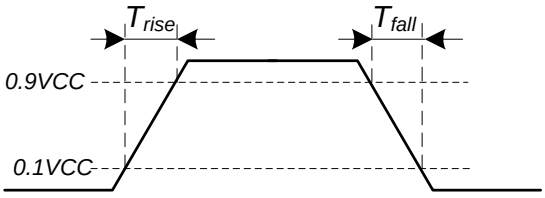

Figure 3: Input signals timing

Output signals rising/falling edges depends on additional capacitance connected to these pin at integration level. The formula of slopes is

$$Time = K_{load}*(C_{routing}+20fF),$$

where 20 fF comes from intrinsic capacitance, $C_{routing}$ is routing capacitance and K_{load} is as follows:

	K_{load}, ns/pF	
	rise	fall
Typical value	1.25	0.91

7.2 PLACEMENT AND ROUTING

PLL is a mixed signal block, which is sensitive to power supply, ground and substrate noise. So, the following recommendations are given.

1. PLL layout can be rotated and flipped in axis X and Y
2. Use separate 1.2V power supply with other highly switching and noisy circuits (if possible) and place 0.25—0.5 nF or more capacitance vcc-gnd around the block
3. Power supply (pin vcc) and ground (pin gnd) wires must allow flowing of 2 mA DC, 4 mA peak currents and should have resistance of less than 1 Ohm
4. Locate block with reference current close to CP_i1uA pin
5. Pitch between LO output path and other noisy paths should be more than 7um or at least 2 um to other paths up to the first sharing buffer. No shielding for this path
6. Use shielding metal for covering CP_i1uA input path
7. IP should be used in 1.2 V voltage domain
8. No routing is allowed over the block

7.3 LAYOUT VERIFICATION

- DRC and LVS are run using Mentor Graphics Calibre
- No dummy structures are required for layers PO, OD, M1—M4

8 OPERATING CHARACTERISTICS

8.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS 65 nm
Status silicon proven
Area 0.009 mm^2

8.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.1 ÷ 1.3 V and T_j = -40 ÷ +85 °C. Typical values are at V_{cc} = 1.2 V and T = +27° C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	1.1	1.2	1.3	V
Temperature range	T_j	-	-40	27	85	ºC
Output frequency	F_{out}	-	50	-	800	MHz
LO duty cycle	LO_{DC}	-	40	50	60	%
Phase noise	LO_{PN}	at 1 MHz	-	-97	-	dBc/Hz
Reference current	I_{ref}	Source from power	0.72	0.85	1.0	uA
Reference frequency	F_{ref}	-	4	6	30	MHz
Ref_clk duty cycle	Ref_clk_{DC}	-	40	50	60	%
VCO control voltage	V_{ctrl}	-	0.2	-	1.0	V
Comparison frequency	F_{comp}	-	4	-	15	MHz
N dividing ratio	N	-	16	-	511	-
C dividing ratio	C	-	1	-	8	-
R dividing ratio	R	-	1	-	2	-
Lock time	T_{lock}	-	-	17	30	us
Lock detector accuracy	S_{err}	-	15	20	25	ns
Lock detector frequency accuracy	F_{err}	-	10	12	16	MHz
Lock monitoring period	MP	$T_{comp} = 1/ F_{comp}$	-	$32*T_{comp}$	-	us
Current consumption	I_{cc}	F_{out} = 400 MHz	160	210	250	uA
		F_{out} = 800 MHz	350	410	450	
Current consumption in standby mode	I_{stb}	-	-	0.03	2.7	uA
Reference signal - high level	V_{RefH}	CMOS	$0.8V_{cc}$	-	1.3	V
Reference signal - low level	V_{RefL}		-0.1	-	0.2	
Input logic - high level	V_{IH}	For digital inputs	$0.8V_{cc}$	-	1.3	V
Input logic - low level	V_{IL}		-0.1	-	0.2	

9 TYPICAL OPERATING CHARACTERISTICS

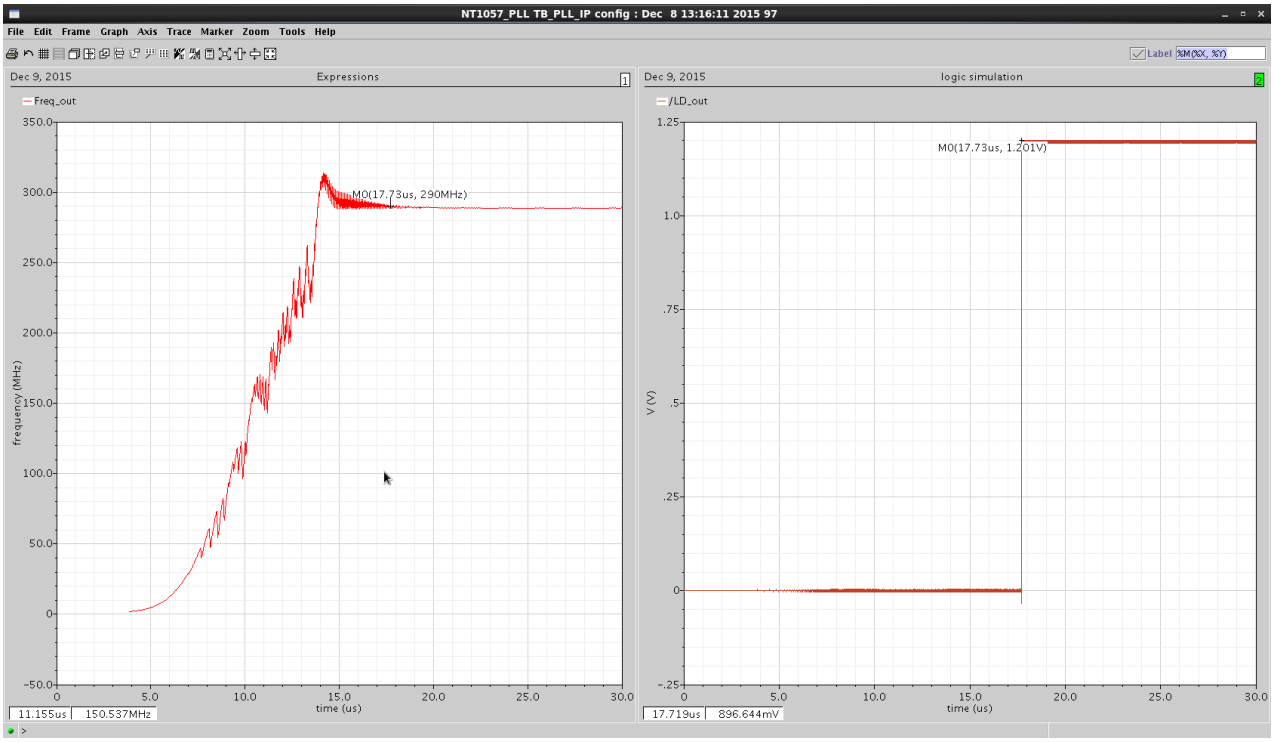

Figure 4: PLL output frequency lock

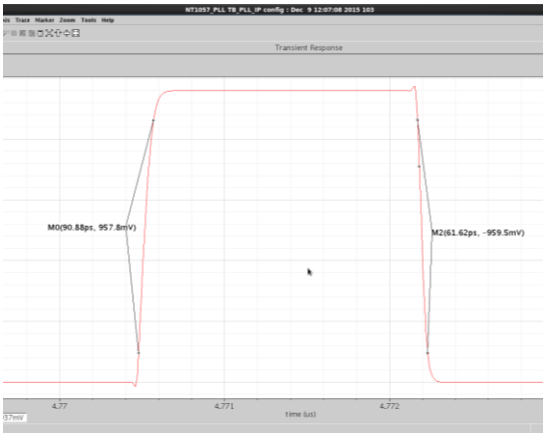

Figure 5: PLL output signal edges with F_{LO} = 288.756 MHz and C_{load} = 70fF

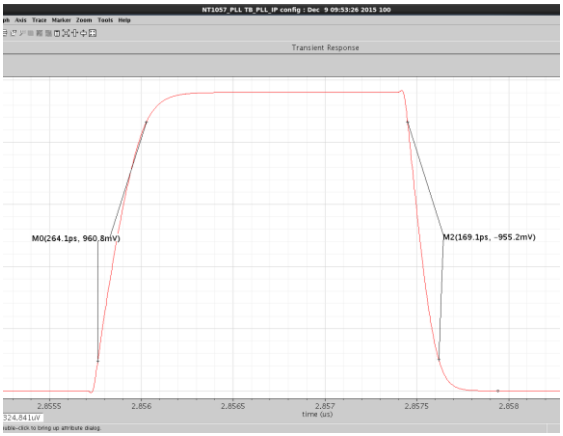

Figure 6: PLL output signal edges with F_{LO} = 288.756 MHz and C_{load} = 220fF

10 DELIVERABLES

Depending on license type, IP may include:

- Schematic or NetList
- Layout or blackbox
- Verilog, lef and lib files
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.1:

- Section 4 Figure updated:
  - CP_i1uA direction added
  - External filtering capacitance vcc-gnd added
  - Pin name RefClk changed to Ref_clk
- Section 5 updated
  - Pins vcc and gnd direction and descriptions updated
  - Pin direction note added
- Section 6.3 added
- Section 7.2 updated
- Section 8.2 updated
  - LO duty cycle parameter added
  - LO phase noise at 1 MHz parameter added
  - Ref_clk duty cycle parameter added
  - Comparison frequency parameter added
  - Lock monitoring period parameter added
  - Lock detector frequency accuracy parameter added
- Section 9.2 updated
  - PLL output signal edges for different C_{load} added
- Section 10 updated

From version 1.0:

- Section 3 updated
- Section 4 Figure updated:
  - Pin name vcc12 changed to vcc
- Section 5 updated
- Section 6.1 added
- Section 7 added
- Section 8.2 Table updated:
  - Reference current value was added
  - Lock time value was added
  - Reference signal high and low levels values were added
- Section 9 added