

## 1 – 600 MHz frequency synthesizer

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### SPECIFICATION

#### 1 FEATURES

- TSMC CMOS 90 nm
- Reference frequency 6 MHz
- Output frequency 1 - 600 MHz
- Supply voltage 1 V
- Working supply current 1 mA
- Portable to other technologies (upon request)

#### 2 APPLICATIONS

- Data transmission systems
- Clock subsystems
- Measurement equipment

#### 3 OVERVIEW

The synthesizer produces stable clock signal in range from 1 to 600MHz. PLL with integer factors of the frequency division is used for synthesis.

External reference clock 6 MHz connects with `pll_iclk` input. The output of the frequency synthesizer forms a stable signal with a frequency from 1 to 600 MHz. The range of possible frequencies is set by the dividing ratio control register `pll_cfg<9:0>` and output frequency is the register value in Mhz. The synthesizer is OFF if value register is 000h.

The device is designed with TSMC CMOS 90 nm technology.

## 4 BLOCK-DIAGRAM

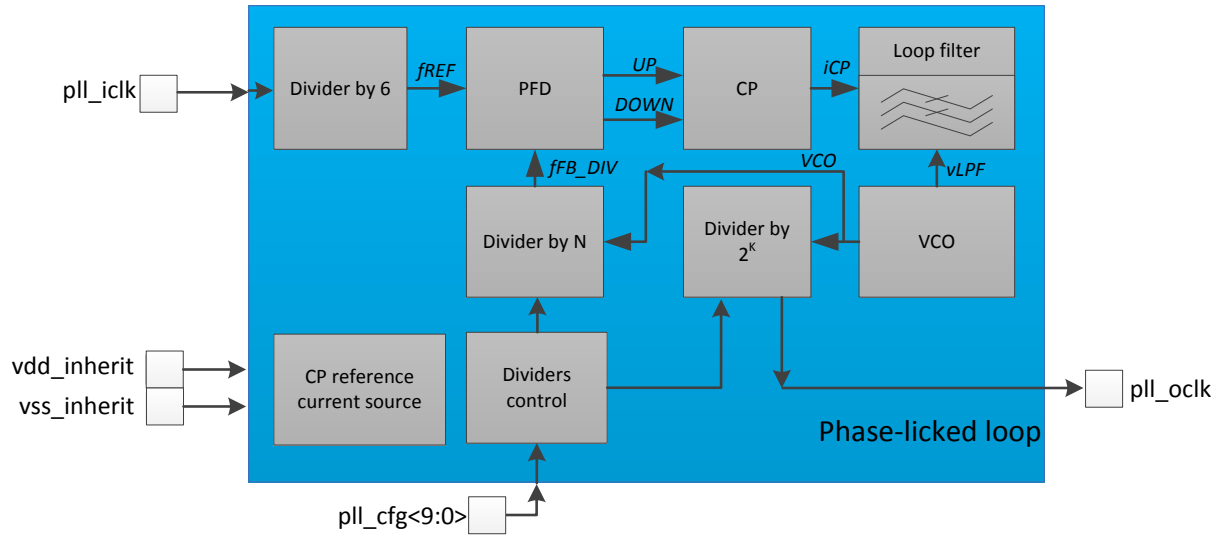


Figure 1: Synthesizer block diagram

## 5 PIN DESCRIPTION

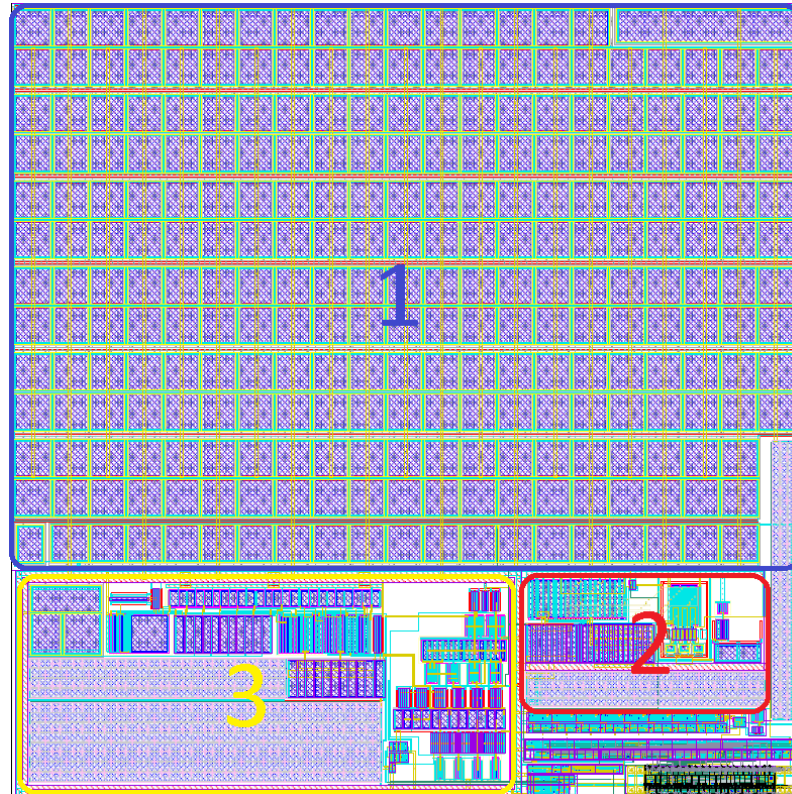
<b>Name</b>	<b>Type</b>	<b>Description</b>
pll_iclk	I	Clock input
pll_cfg<9:0>	I	Frequency divisor register (for synthesizer's feedback)
pll_oclk	O	Synthesizer output
vdd_inherit	I/O	Supply voltage, 1.0 V
vss_inherit	I/O	Ground

## 6 LAYOUT DESCRIPTION

Table 1 shows the dimensions of the block synthesizer.

**Table 1:** Dimensions.

Dimensions	Value	Unit
Height	222	um
Width	219	um



**Figure 2:** Synthesizer's layout view

1. Low pass filter
2. Voltage control oscillator
3. Charge pump and current reference circuits

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ TSMC CMOS 90 nm  
 Status \_\_\_\_\_ pre-silicon verification  
 Area \_\_\_\_\_ 0.05 mm<sup>2</sup>

### 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{dd}=0.9 \div 1.1$  V and  $T_j=-40 \div +95^\circ\text{C}$ , unless otherwise specified; typical values are  $V_{dd}=1.0$  V and  $T_j = +27^\circ\text{C}$ .

Parameter	Symbol	Condition	Value			Unit
			min	type	max	
Supply voltage	$V_{dd}$	-	0.9	1.0	1.1	V
Current consumption	$I_{en}$	-	-	-	1	mA
Standby mode current consumption	$I_{st}$	-	-	-	1	uA
Power dissipation	$W_{dd}$	-	-	-	1.1	mW
Operating temperature range	$T_j$	-	-40	27	95	°C
Clock frequency	$F_{pll\_iclk}$	-	-	6	-	MHz
Synthesized frequency	$F_{pll\_oclk}$	-	1	-	600	MHz
Instantaneous change in frequency of the output signal	$J_{pll\_oclk}$	$F_{pll\_oclk} = 600$ MHz	-	-	0.2	MHz
Input high level voltage	$V_{IH}$	For digital inputs	0.7	-	-	V
Input low level voltage	$V_{IL}$		-	-	0.3	V

## 8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation