Phase-locked loop system

SPECIFICATION

1 FEATURES

- SMIC CMOS 0.18µm
- Wide frequency range (2.8…3.3 GHz)
- Built-in switched capacitors sections for VCO frequency adjustment
- Low noise figure
- High lock detector accuracy
- Charge pump low output current disbalance
- Low current consumption
- Low power consumption
- No external components required
- Small area
- Portable to other technologies (upon request)

2 APPLICATION

- Portable transmitters
- Portable transceiver

3 OVERVIEW

PLL is an automatic control system adjusting controlled oscillator frequency to be equal to reference oscillator frequency multiplied by a given integer. Frequency adjustment is carried out by using negative feedback. A phase detector compares a controlled oscillator output with a reference signal. The result is a charge pump current output that supplies external feedback filter and converted to a voltage for controlled oscillator adjustment.
Clock divider is used to generate signals with specified frequency. Delta-sigma modulator makes it possible to operate with reference oscillator of different frequency.
The block is fabricated on SMIC CMOS 0.18µm technology.

4 STRUCTURE

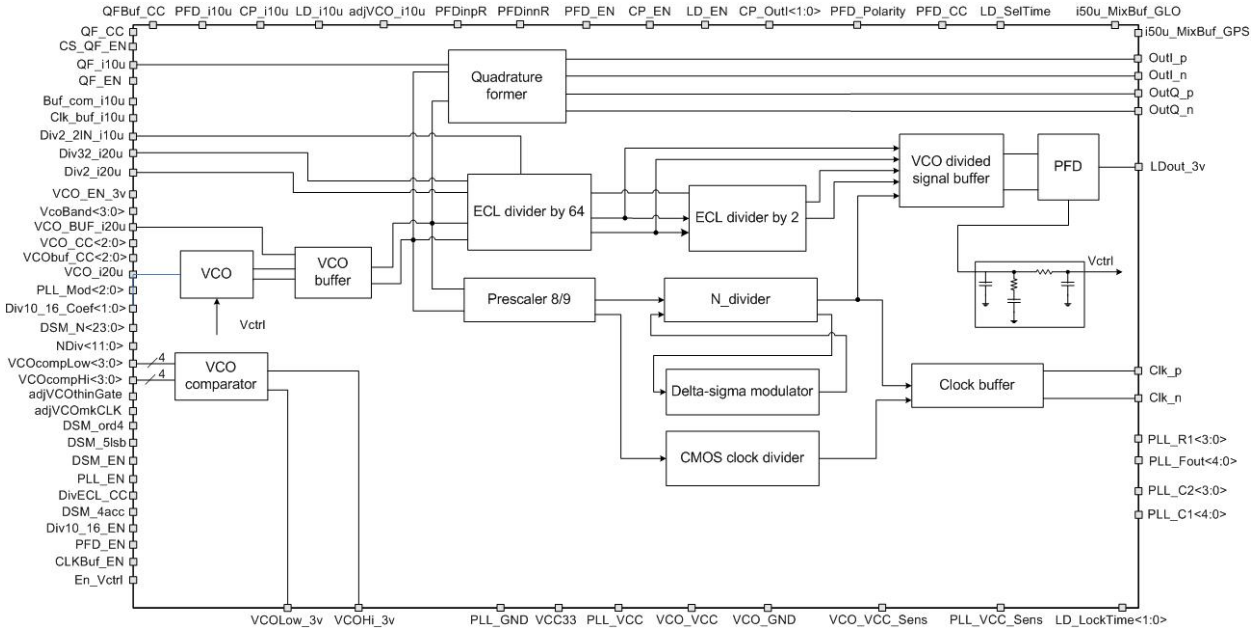

Figure 1: Phase-locked loop system structure

5 PIN DESCRIPTION

Name	Direction	Description
QF_ i10u	I	Quadrature former reference current (10 µA)
Clk_buf_i10u	I	Reference current of reference frequency buffer (10µA)
Buf_com_i10u	I	Reference current of VCO divided signal buffer (10µA)
CP_i10u	I	Charge pump reference current (10µA)
PFD_i10u	I	PFD reference current (10µA)
VCO_i20u	I	VCO core reference current (20 µA)
VCO_BUF_i20u	I	VCO buffer reference current (20 µA)
adjVCO_i10u	I	Reference current VCO comparator
Div2_2IN_i10u	I	ECL divider by 2 reference current (10 µA)
Div32_i20u	I	ECL divider by 64 reference current (20 µA)
Div2_i20u	I	
LD_i10u	I	Lock detector reference current (10µA)
Vctrl	I	VCO control voltage input
PFDinpR	I	PFD differential input
PFDinnR	I	
VCO_EN_3v	I	VCO enable/disable
PFD_EN	I	VCO divided signal buffer enable/disable
PLL_EN	I	PLL enable/disable
QF_EN	I	Quadrature former enable/disable
Div_10_16_EN	I	CMOS clock divider enable/disable
DSM_EN	I	Delta-sigma modulator enable/disable

Table “Pin Description” (continue)

Name	Direction	Description
LD_EN	I	Lock detector enable/disable
CLKBuf_EN	I	Clock buffer enable/disable
PFD_Polarity	I	PFD polarity
En_Vctrl	I	VCO control voltage
VCO_CC<2:0>	I	VCO core current selection
VCObuf_CC<1:0>	I	Buffer current selection
DivECL_CC	I	ECL frequency divider by 64 current control
CP_OutI<1:0>	I	Charge pump output current control
PFD_CC	I	PFD current control
QF_CC	I	Quadrature former current control
QFBuf_CC	I	Quadrature former buffer current control
VCOcompHi<3:0>	I	Voltage detector upper bound (VCO subband autoselect system)
VCOcompLow<3:0>	I	Voltage detector lower bound (VCO subband autoselect system)
VcoBand<3:0>	I	Switching capacitor sections
QF_CS_TD	I	Quadrature former temperature dependent source enable
NDiv<11:0>	I	Delta-sigma modulator integer dividing ratio
Div10_16_Coef<1:0>	I	Dividing ratio of CMOS clock divider
LD_LockTime<1:0>	I	Detection period adjustment
LD_SelTime	I	Detection accuracy adjustment
PLL_Mod_3v<2:0>	I	PLL mode select
adjVCOmkCLK	I	Voltage detector bounds type (VCO subband autoselect system)
adjVCOthinGate	I	Fixed bounds mode control
DSM_ord4	I	Selection of 4th order delta-sigma modulator signal
DSM_4acc	I	All four accumulators are set to non-zero value
DSM_5lsb	I	First 5 bits of first accumulator are set “1”
DSM_N<23:0>	I	DSM fractional dividing ratio
PLL_C1<4:0>	I	PLL feedback filter adjustment
PLL_C2<3:0>	I	
PLL_R1<3:0>	I	
PLL_Fcut<4:0>	I	
VcoHi_3v	O	VCO maximum required control voltage indicator
VcoLow_3v	O	VCO minimum allowable control voltage indicator
LDout_3v	O	Lock detector output
CLK_n	O	Clock buffer differential output
CLK_p	O	
i50u_MixBuf_GLO	O	Reference current of the 1st channel mixer buffer
i50u_MixBuf_GPS	O	Reference current of the 2nd channel mixer buffer
OutI_p	O	Quadrature former buffer differential outputs
OutI_n	O	
OutQ_p	O	
OutQ_n	O	

Table “Pin Description” (continue)

Name	Direction	Description
VCC33	IO	High level supply voltage
VCO_VCC	IO	VCO supply voltage
VCO_VCC_Sens	IO	VCO supply voltage feedback
PLL_VCC	IO	PLL supply voltage
PLL_VCC_Sens	IO	PLL supply voltage feedback
VCO_GND	IO	VCO ground
PLL_GND	IO	PLL ground

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	647.46	µm
Width	1436.16	µm

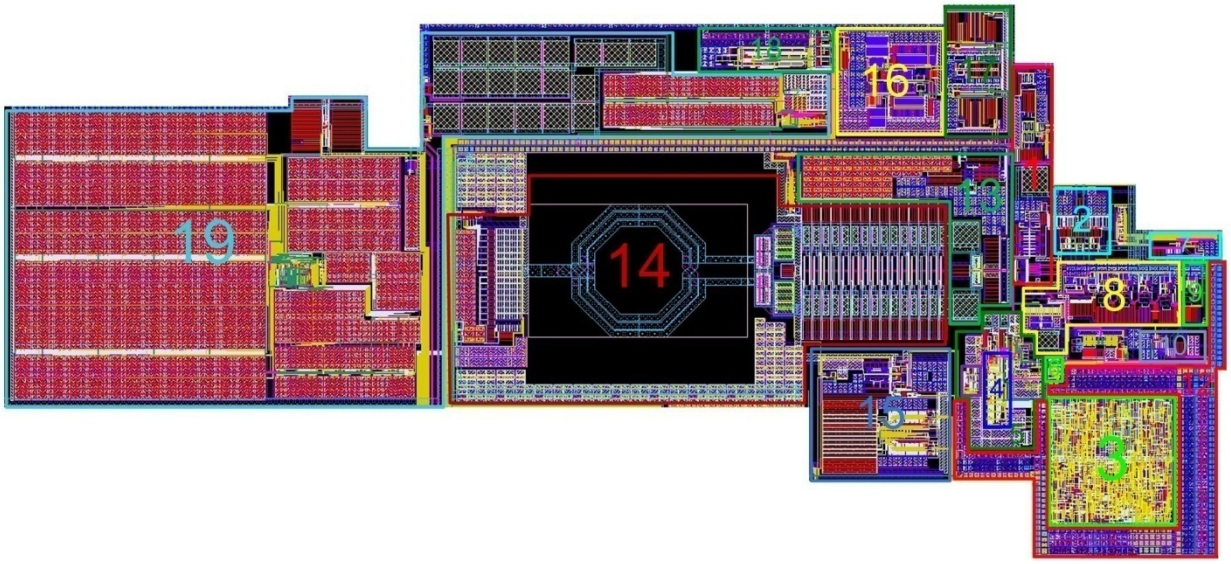

Figure 2: Device layout view

1. Quadrature former
2. Quadrature former buffer
3. Delta-sigma modulator
4. N-divider
5. Prescaler 8/9
6. CMOS commutator
7. Buffer of VCO divided signal
8. ECL frequency divider by 64
9. ECL frequency divider by 2
10. Clock buffer
11. CMOS clock divider
12. Filtering capacitors
13. VCO buffer
14. VCO
15. VCO comparator
16. Charge Pump
17. ECL PFD
18. Lock detector
19. Feedback filter

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ SMIC CMOS 0.18 µm
Status _____ silicon proven
Area _____ 0.6 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.7 ÷ 1.9 V and T = -45 ÷ +85 °C. Typical values are at V_{cc} = 1.8 V and T = 27° C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	1.7	1.8	1.9	V
Operating temperature range	T	-	-45	27	85	°C
PLL dividing ratio	N_{PLL}	-	56	-	16383	-
Clock frequency	F_{clk}	-	-	49.68	-	MHz
Reference frequency	F_r	-	-	24.84	-	MHz
Oscillation frequency range	F_{Osc}	-	2.8	-	3.3	GHz
Peak-to-peak output voltage	A_{VCO}	Differential output	742	-	-	mV
Peak-to-peak at clock frequency differential outputs	A_{cmos}	CMOS	1.7	1.8	1.9	V
		Differential output	0.3	0.32	0.45	
R divider programmable values	R_{PLL}	-	1	-	32	-
Comparison frequency range	F_{PFD}	-	-	24.84	-	MHz
Lock monitoring time	Sel_time	-	2.58	-	20.6	µs
Lock accuracy	Prec_lock	Preset 1	6.5	7	7.5	ns
		Preset 2	13	14	15	
Current consumption in an active mode	I_{cc}	-	5.5	7.2	8.75	mA
Current consumption in a standby mode	I_{stb}	-	-	75	-	nA
Oscillator phase noise spectral concentration	I_s	at 10kHz offset	-	-83	-80	dBHz
Input logic-high level	V_{IH}	For digital inputs	0.7 V_{cc}	-	3.6	V
Input logic-low level	V_{IL}		-0.25	-	0.3	V

Table 2: Preset description.

Preset	Control signal
Preset 1	LD_SelErr=”0”
Preset 2	LD_SelErr=”1”

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

1. From version 1.0:
   - Table “Electrical characteristics” (refer to page 6).