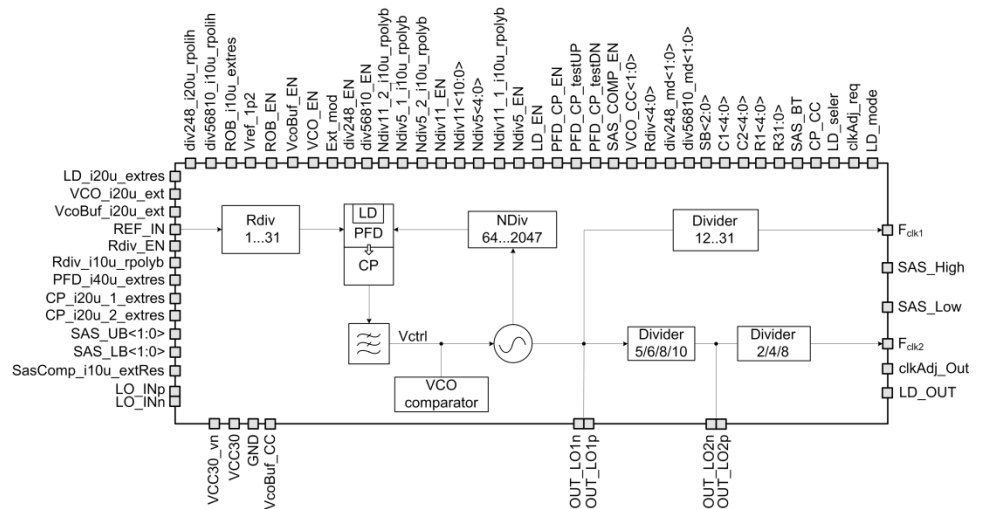


1.68 to 1.917 GHz Phase-Locked Loop

OVERVIEW

Frequency synthesizer built on PLL by dividing the integer coefficients. Synthesizer unit includes: R-divider of external reference oscillator frequency with a programmable division factor of 1 to 31, frequency-phase detector (PFD) with the charge pump, loop filter, a voltage controlled oscillator (VCO), VCO voltage control comparators, VCO frequency divider with programmable dividing ratio of 12 to 31, VCO frequency N-divider with programmable dividing ratio of 64 to 2047, 5/6/8/10 divider, 2/4/8 divider.



IP technology: AMS SiGe BiCMOS 0.350um.

IP status: silicon proven.

Area: 0.3mm²

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V _{cc}	-	2.85	3.0	3.15	V
Operating temperature range	T _j	-	-60	27	+85	°C
1 st oscillator frequency range	F _{LO1}	-	1692	1769	1973	MHz
2 nd oscillator frequency range	F _{LO2}	-	175	-	225	MHz
1 st oscillator peak-to-peak output voltage	A _{VCO}	Differential output	360	420	500	mV
PLL division ratio	N _{PLL}	-	64	-	2047	-
Reference frequency	F _{ref}	-	10	12.8	125	MHz
Reference frequency divider ratio	R _{PLL}	-	1	-	31	-
VCO phase noise at 1 MHz offset	PN _{VCO}	-	-	-	-119	dBc/Hz
Clock frequency	F _{CLK}	-	10	-	125	MHz
Clock frequency output voltage	A _{CLK}	Differential signal	460	-	700	mV
DC clock frequency output voltage	V _{DC_CLK}	Normal mode	-	V _{cc} -0.12	-	V
		LVDS mode	-	V _{cc} -1.75	-	V
Frequency synthesizer current consumption	I _{cc}	-	-	20.8	24.5	mA
Frequency synthesizer stand-by mode	I _{stby}	-	-	7	500	nA
Clock buffer current consumption in an active mode	I _{ccCLK}	-	1.6	1.8	2	mA
Clock buffer current consumption in stand-by mode	I _{stbyCLK}	-	-	3	100	nA
Input logic-level high	V _{IH}	For digital inputs	0.7V _{cc}	-	V _{cc} +0.3	V
Input logic-level low	V _{IL}		-	-	0.3V _{cc}	V