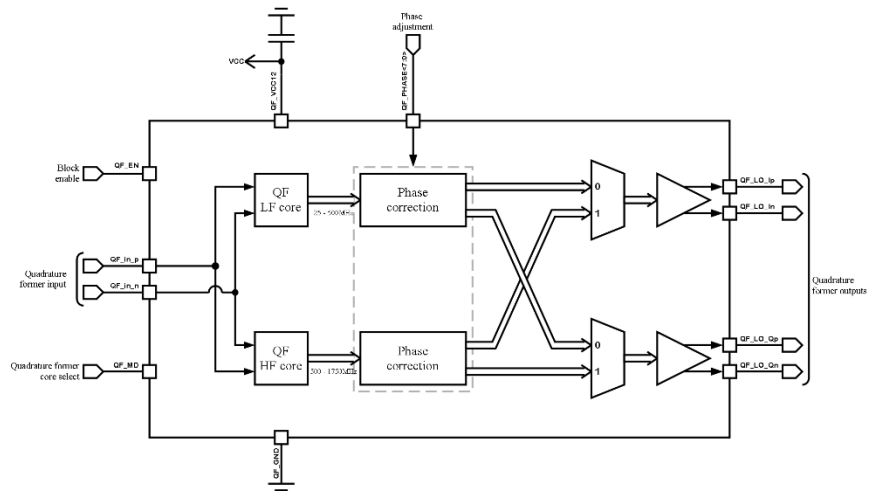


## Quadrature former 25-1750MHz

### OVERVIEW

The quadrature former block is intended to generate quadrature signal in frequency range 25-1750MHz with phase correction  $\pm 4^\circ$ . The quadrature former core is based on frequency division by 4, implemented on CMOS logic. The block input frequency range 100-7000MHz. The phase correction block uses the dependence of the fronts rise rate of the supply voltage, that in turn affects the phase of the output quadrature signal. The buffers located at the output of the quadrature former, in addition to the output power amplifying, also serve as a junction between the core (frequency divider) and the external blocks. IP technology: TSMC CMOS 55nm; IP status: silicon proven; Area: 0.0348mm<sup>2</sup>.



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### ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit	
			min	typ.	max		
Supply voltage	V <sub>CC</sub>	-	1.08	1.20	1.32	V	
Operating temperature range	T <sub>J</sub>	Nominal	-45	+25	+85	°C	
Current consumption	I <sub>CC</sub>	Operating mode	F <sub>OUT</sub> = 25MHz	-	0.02	-	mA
			F <sub>OUT</sub> = 500MHz	-	0.5	-	
			F <sub>OUT</sub> = 1750MHz	-	1.3	-	
		Standby mode	-	0.3	8	µA	
		Power-off mode	-	0.1	0.3	nA	
QF division ratio	N	-	-	4	-	-	
Input frequency range	F <sub>IN</sub>	mode 1	100	-	2000	MHz	
		mode 2	2000	-	7000		
Output frequency range	F <sub>OUT</sub>	mode 1	25	-	500	MHz	
		mode 2	500	-	1750		
Phase adjustment range	Δφ (delta)	F <sub>OUT</sub> = 125MHz, mode 1	-	0.25	-	degree	
		F <sub>OUT</sub> = 500MHz, mode 1	-	4	-		
		F <sub>OUT</sub> = 1250MHz, mode 2	-	5	-		
		F <sub>OUT</sub> = 1750MHz, mode 2	-	16	-		
Phase adjustment accuracy	dφ	F <sub>OUT</sub> = 125MHz, mode 1	-	0.001	-	degree	
		F <sub>OUT</sub> = 500MHz, mode 1	-	0.016	-		
		F <sub>OUT</sub> = 1250MHz, mode 2	-	0.02	-		
		F <sub>OUT</sub> = 1750MHz, mode 2	-	0.07	-		
Input logic-level low	V <sub>IL</sub>	For digital inputs	0	-	0.1	V	
Input logic-level high	V <sub>IH</sub>		V <sub>CC</sub> -0.1	-	V <sub>CC</sub> +0.1	V	