# Quadrature former 75-750 MHz

## SPECIFICATION

## 1 FEATURES

- TSMC CMOS 65 nm
- Output frequency range 75-750 MHz
- Input signal division (by 8, 16, 32 or 64)
- High accuracy of the phase control
- Operating-temperature range: from -40 °C to + 125 °C
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

## 2 APPLICATION

- Quadrature signal processing for mixer

## 3 FUNCTIONAL DESCRIPTION

This device is designed to generate a quadrature heterodyne (oscillator) signal. CML logic quadrature generator consists of pre-switchable divider with the division factor 1, 2, 4, 8, divider by 2, divider by 4 that form quadrature signal, output signal (to the input) strobbing block, and phase adjustment block implemented on signal delay time.

## 4 STRUCTURE

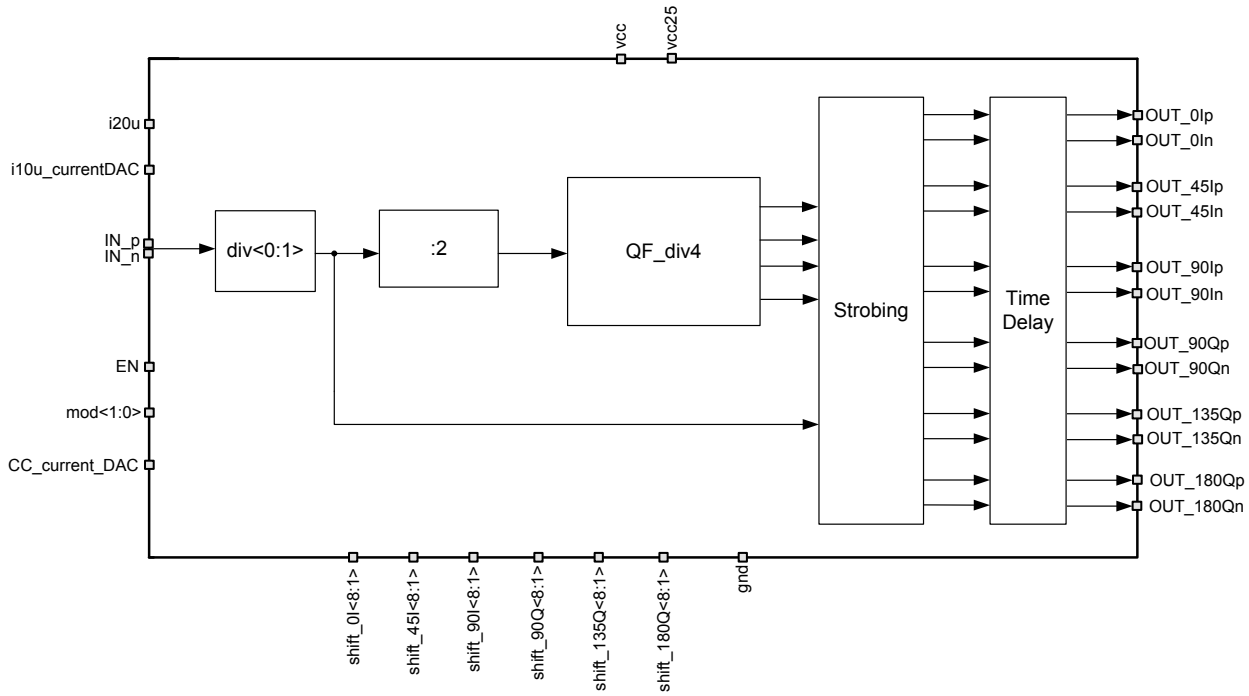


Figure 1: Quadrature former 75-750 MHz structure.

# 5 PIN DESCRIPTION

| Name | Direction | Description |
|---|---|---|
| i20u | IO | Reference current 20 µA |
| i10u_currentDAC | IO | Reference current 10 µA |
| EN | I | QF enable quadrature former |
| mod<1:0> | I | Divider mode |
| shift_0I<8:1> | I | Phase correction control |
| shift_45I<8:1> | I | |
| shift_90I<8:1> | I | |
| shift_90Q<8:1> | I | |
| shift_135Q<8:1> | I | |
| shift_180Q<8:1> | I | |
| CC_DAC | I | DAC current consumption control |
| IN_p | I | Differential input |
| IN_n | I | |
| OUT_0Ip | O | I+ channel differential output |
| OUT_0In | O | |
| OUT_45Ip | O | I0 channel differential output |
| OUT_45In | O | |
| OUT_90Ip | O | I- channel differential output |
| OUT_90In | O | |
| OUT_90Qp | O | Q- channel differential output |
| OUT_90Qn | O | |
| OUT_135Qp | O | Q0 channel differential output |
| OUT_135Qn | O | |
| OUT_180Qp | O | Q+ channel differential output |
| OUT_180Qn | O | |
| vcc25 | IO | Supply voltage 2.5 V |
| vcc | IO | Supply voltage 1.2 V |
| gnd | IO | Ground |

# 6 LAYOUT DESCRIPTION

The block dimensions are given in table 1.

Table 1: Block dimensions.

| Dimension | Value | Unit |
|---|---|---|
| Height | 230 | µm |
| Width | 600 | µm |

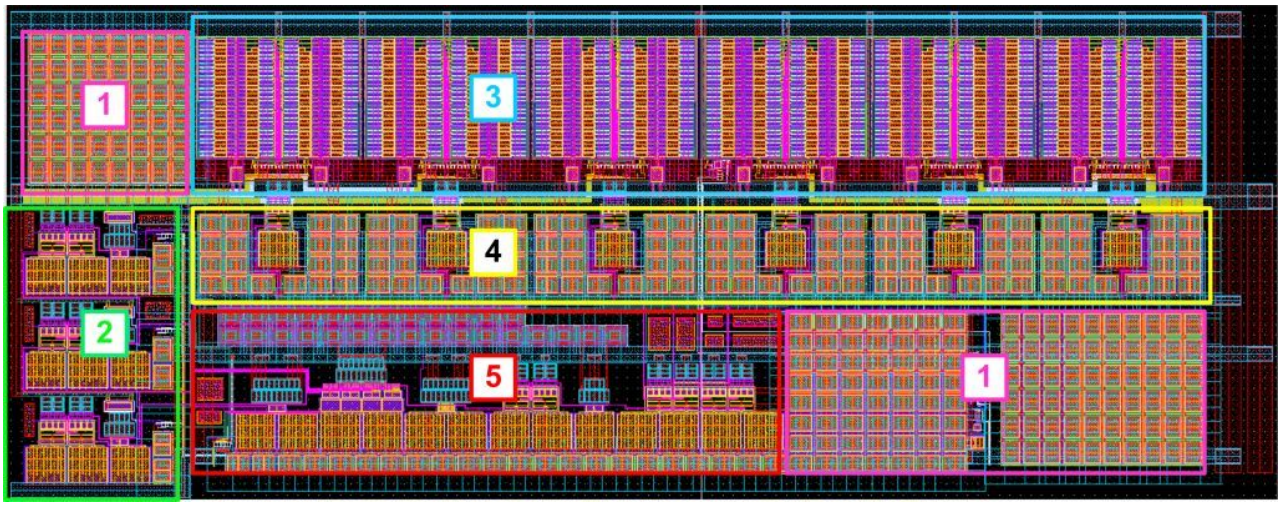


Figure 2: Quadrature former 75-750 MHz layout view.

1. Capacitors
2. Divider
3. Time delay
4. Strobing
5. QF and divider by 2

# 7 OPERATING CHARACTERISTICS

## 7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC CMOS 65 nm
Status _____ silicon proven
Area _____ 0.014 $mm^2$

## 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{cc}$ = 1.14 ÷ 1.26 V and T = -40 ÷ 125 °C. Typical values are at $V_{cc}$ = 1.2 V and T = 85 °C, unless otherwise specified.

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | type | max | |
| Supply voltage | $V_{cc}$ | - | 1.14 | 1.2 | 1.26 | V |
| Temperature range | T | - | -40 | +85 | +125 | °C |
| Input frequency range | $F_{in}$ | - | 3.0 | - | 6.0 | GHz |
| Output frequency range | $F_{out}$ | - | 75 | - | 750 | MHz |
| Input frequency division ratio | N | mod= “00” | - | 8 | - | - |
| | | mod= “01” | - | 16 | - | |
| | | mod= “10” | - | 32 | - | |
| | | mod= “11” | - | 64 | - | |
| Output amplitude | $V\_out_{p-p}$ | - | - | 0.5 | - | V |
| Input amplitude | $V\_in_{p-p}$ | - | 0.5 | - | - | V |
| IQ phase error | φ | - | - | - | ±2 | degree |
| Phase adjustment range | $\varphi_{corr.}$ | - | | - | ±5 | degree |
| Current consumption | I_av | - | - | 15 | 17 | mA |
| Input logic-level high | $V_{IH}$ | For digital inputs | $0.85V_{cc}$ | - | $V_{cc}$ | V |
| Input logic-level low | $V_{IL}$ | | -0.1 | - | +0.1 | V |

# 8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation