Quadrature former 0.75-3 GHz

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- Output frequency range 0.75-3 GHz
- Input signal division (by 2 or 4)
- High accuracy of the phase control
- Operating-temperature range: from -40 °C to + 125 °C
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- Quadrature signal processing for mixer

3 OVERVIEW

This device is designed to generate a quadrature heterodyne signal.CML logic quadrature generator consists of divider by 2 or 4 that form quadrature. MUX to select the one is running, and phase adjustment block implemented on signal delay time.

4 STRUCTURE

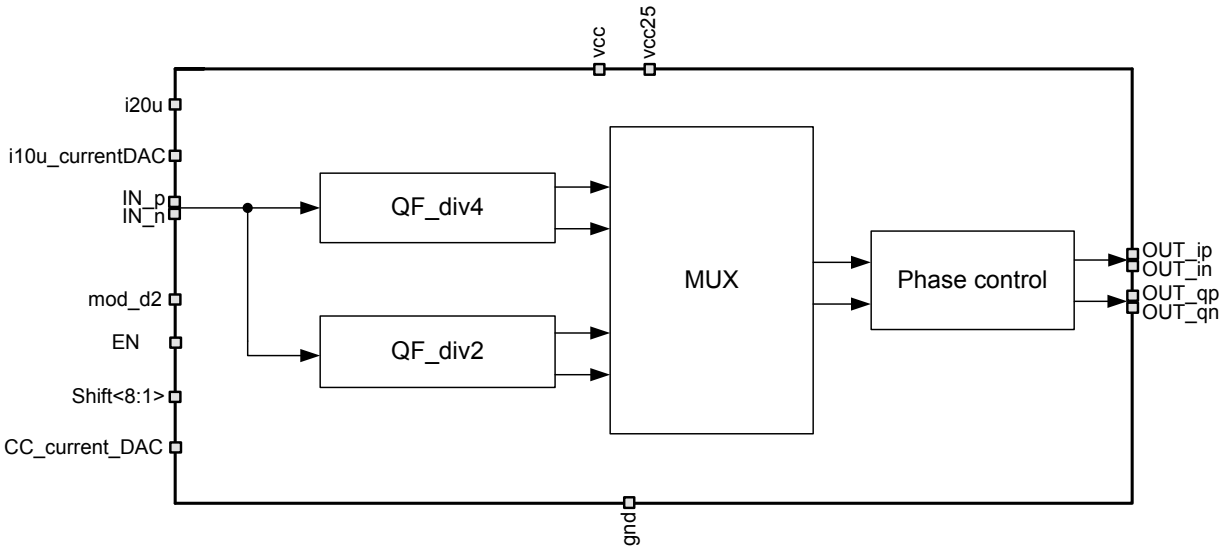

Figure 1: Quadrature former 0.75-3 GHz structure.

5 PIN DESCRIPTION

Name	Direction	Description
i20u	IO	Reference current 20 µA
i10u_currentDAC	IO	Reference current 10 µA
EN	I	QF enable:
CC_current_DAC	I	DAC current consumption
Shift<8:1>	I	Phase correction control
mod_d2	I	Divider mode
IN_p	I	Differential input
IN_n	I	
OUT_ip	O	I channel differential output
OUT_in	O	
OUT_qp	O	Q channel differential output
OUT_qn	O	
vcc25	I	Supply voltage 2.5 V
vcc	I	Supply voltage 1.2 V
gnd	I	Ground

6 LAYOUT DESCRIPTION

The block dimensions are given in table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	282	µm
Width	180	µm

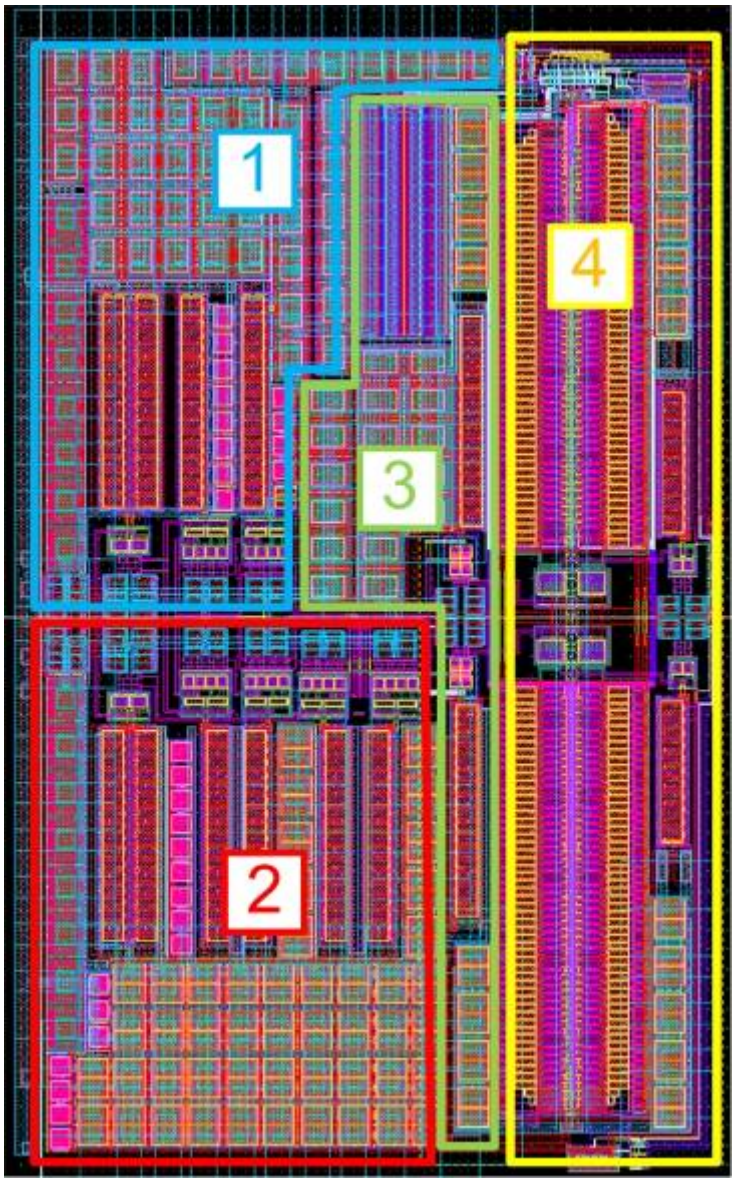

Figure 2: Quadrature former layout view.

1. Divider by 2
2. Divider by 4
3. MUX
4. Phase tuner block

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC CMOS 65 nm
Status _____ silicon proven
Area _____ 0.068 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.14 ÷ 1.26 V, V_{cc25} = 2.375 ÷ 2.625 V and T = -40 ÷ 125 °C. Typical values are at V_{cc} = 1.2 V, V_{cc25} = 2.5 V and T = 85 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	type	max	
Supply voltage	V_{cc25}	-	2.375	2.5	2.625	V
	V_{cc}	-	1.14	1.2	1.26	V
Temperature range	T	-	-40	+85	+125	°C
Input frequency range	F_{in}	-	3.0	-	6.0	GHz
Output frequency range	F_{out}	-	0.75	-	3	GHz
Division ratio	N	Division by 2	-	2	-	-
		Division by 4	-	4	-	
Output amplitude	V_out_{p-p}	-	-	0.5	-	V
Input amplitude	V_in_{p-p}	-	0.5	-	-	V
IQ phase error	φ	-	-	-	±2	degree
Phase adjustment range	$φ_{corr.}$	-	±0.05	-	±5	degree
Current consumption	I_av	-	-	15	17	mA
Input logic-level high	V_{IH}	-	$0.85V_{cc}$	-	$2.45V_{cc}$	V
Input logic-level low	V_{IL}	-	-0.1	-	+0.1	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation