Quadrature former

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- Output frequency range 0.075-3 GHz
- Input frequency division (by 2, 4, 8, 16, 32 or 64)
- High accuracy of the phase control
- Output signal strobbing
- Portable to other technologies (upon request)

2 APPLICATION

- Quadrature signal processing for mixer

3 OVERVIEW

This device is designed to generate a quadrature local oscillator signal. A quadrature generator circuit constructed in CMOS logic and consists of two converters ECL/CMOS, quadrature former with input frequency divider by 2 or 4, prescaler by 2, 4, 8, 16 and phase control block, with ability of fine tuning of output signal phase. To reduce phase noise output triggers are strobbed by high-frequency signal.

4 STRUCTURE

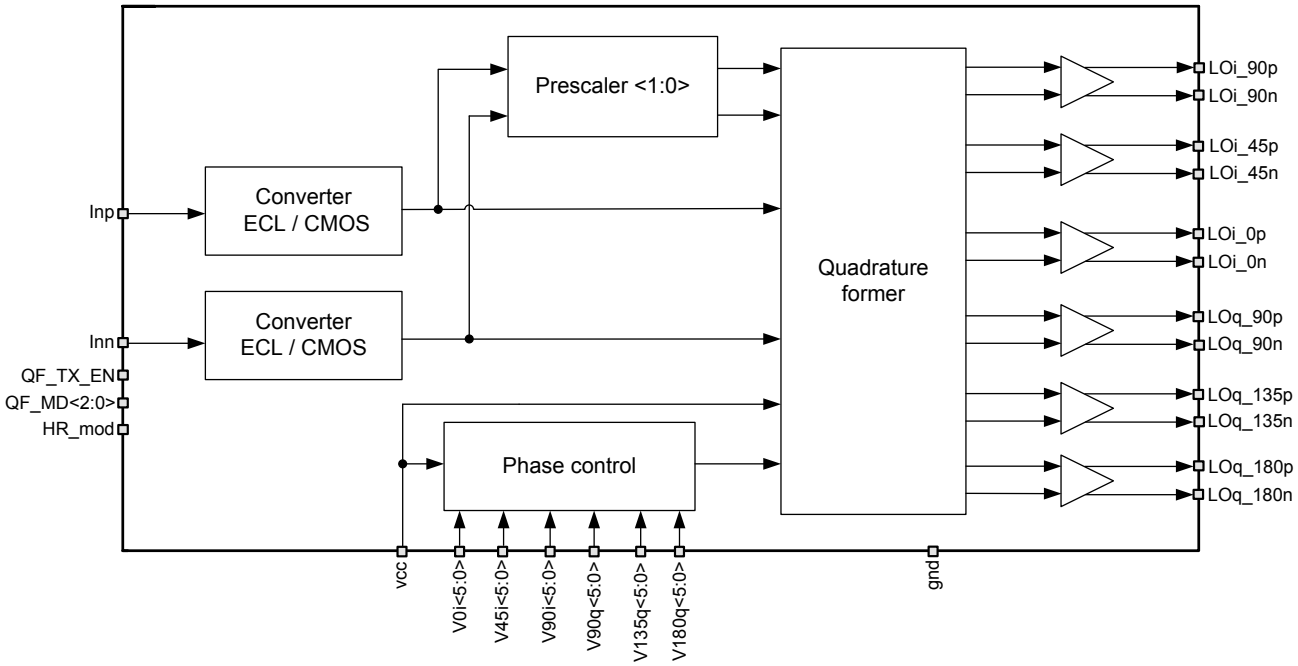

Figure 1: Quadrature former structure

5 PIN DESCRIPTION

Name	Direction	Description
QF_TX_EN	I	Enable/disable QF
QF_MD<2:0>	I	Division ratio selection
HR_mod	I	Quadrature former harmonic rejection mode selection
V0i<5:0>	I	Phase correction control for I- channel
V45i<5:0>	I	Phase correction control for I0 channel
V90i<5:0>	I	Phase correction control for I+ channel
V90q<5:0>	I	Phase correction control for Q- channel
V135q<5:0>	I	Phase correction control for Q0 channel
V180q<5:0>	I	Phase correction control for Q+ channel
Inp	I	Differential input from VCO
Inn	I	
LOi_90p	O	I+ channel differential output
LOi_90n	O	
LOi_45p	O	I0 channel differential output
LOi_45n	O	
LOi_0p	O	I- channel differential output
LOi_0n	O	
LOq_90p	O	Q- channel differential output
LOq_90n	O	
LOq_135p	O	Q0 channel differential output
LOq_135n	O	
LOq_180p	O	Q+ channel differential output
LOq_180n	O	
vcc	IO	Supply voltage 1.2 V
gnd	IO	Ground

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	450	µm
Width	165	µm

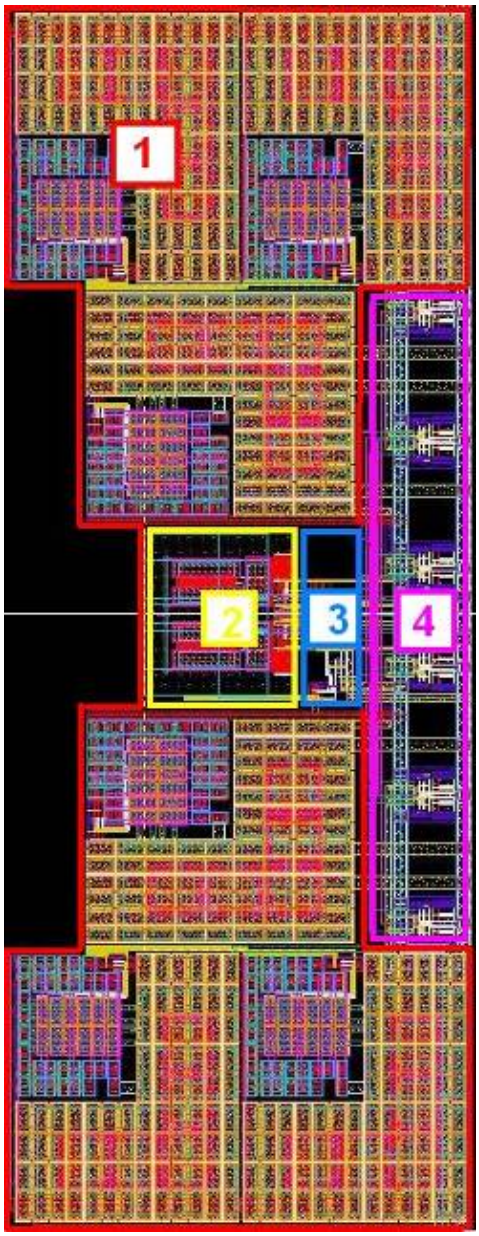

Figure 2: Quadrature former layout view

1. Phase control
2. Converters ECL/CMOS
3. Prescaler and Quadrature former
4. Strobing triggers and amplifying buffers

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC 65 nm CRN65LP
Status _____ silicon proven
Area _____ 0.068 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.14 ÷ 1.26 V and T = -40 ÷ 125 °C. Typical values are at V_{cc} = 1.2 V and T = 85 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	1.14	1.2	1.26	V
Temperature range	T	-	-40	+85	+125	°C
Input frequency range	F_{in}	-	3.0	-	6.0	GHz
Output frequency range	F_{out}	-	0.075	-	3	GHz
Division ratio	N	Division by 2	-	2	-	-
		Division by 4	-	4	-	
		Division by 8	-	8	-	
		Division by 16	-	16	-	
		Division by 32	-	32	-	
		Division by 64	-	64	-	
Output amplitude	V_out_{p-p}	CMOS	-	V_{cc}	-	V
Input amplitude	V_in_{p-p}	-	0.5	-	-	V
IQ phase error	φ	-	-	-	±4	degree
Phase adjustment range	$φ_{corr.}$	-	±0.05	-	±5	degree
Current consumption	I_av	-	-	11	15	mA
Input logic-level high	V_{IH}	-	0.85V_{cc}	-	1.15V_{cc}	V
Input logic-level low	V_{IL}	-	-0.1	-	+0.1	V

8 TYPICAL CHARACTERISTICS

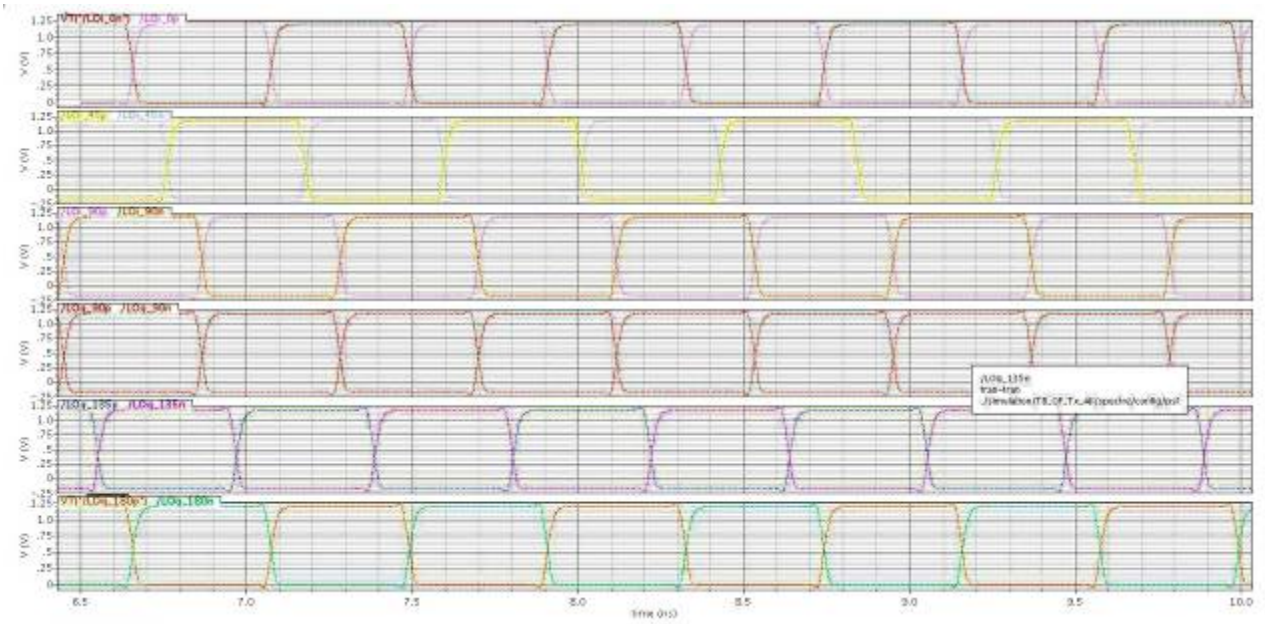

Figure 3: The time diagram of the quadrature former

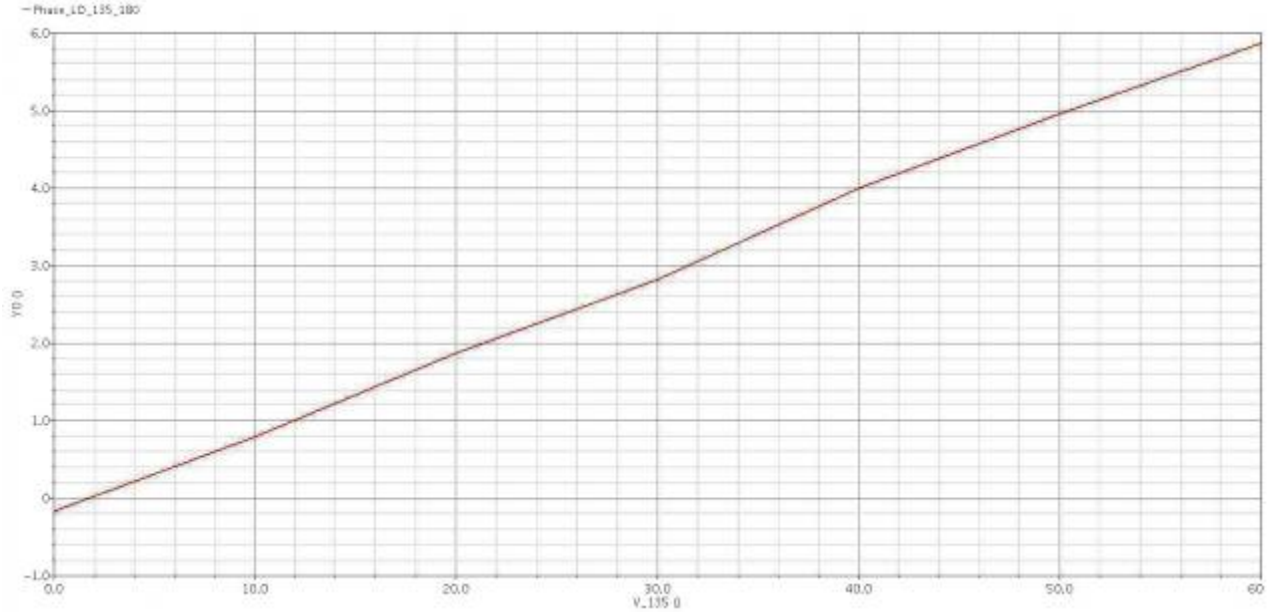

Figure 4: Phase tuning range (heterodyne = 1.5 GHz)

9 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation