Quadrature former

SPECIFICATION

1 FEATURES

- AMS035 BiCMOS 0.35 µm
- 4 independent outputs
- Works with two input signal with different signals for output 1,2 and 3,4 respectively
- Up to 4 outputs with one input signal
- Adjustable output phase in range ±4.5° for each channel
- Portable to other technologies (upon request)

2 APPLICATION

- Receiver

3 OVERVIEW

Quadrature former (QF) generate differential output signals with phase shift of 90° for each of 4 channel, coherent to input signal. QF has two inputs and works with one differential or two independent signals. Output phase adjustment for each channel gives minimal phase error.

4 STRUCTURE

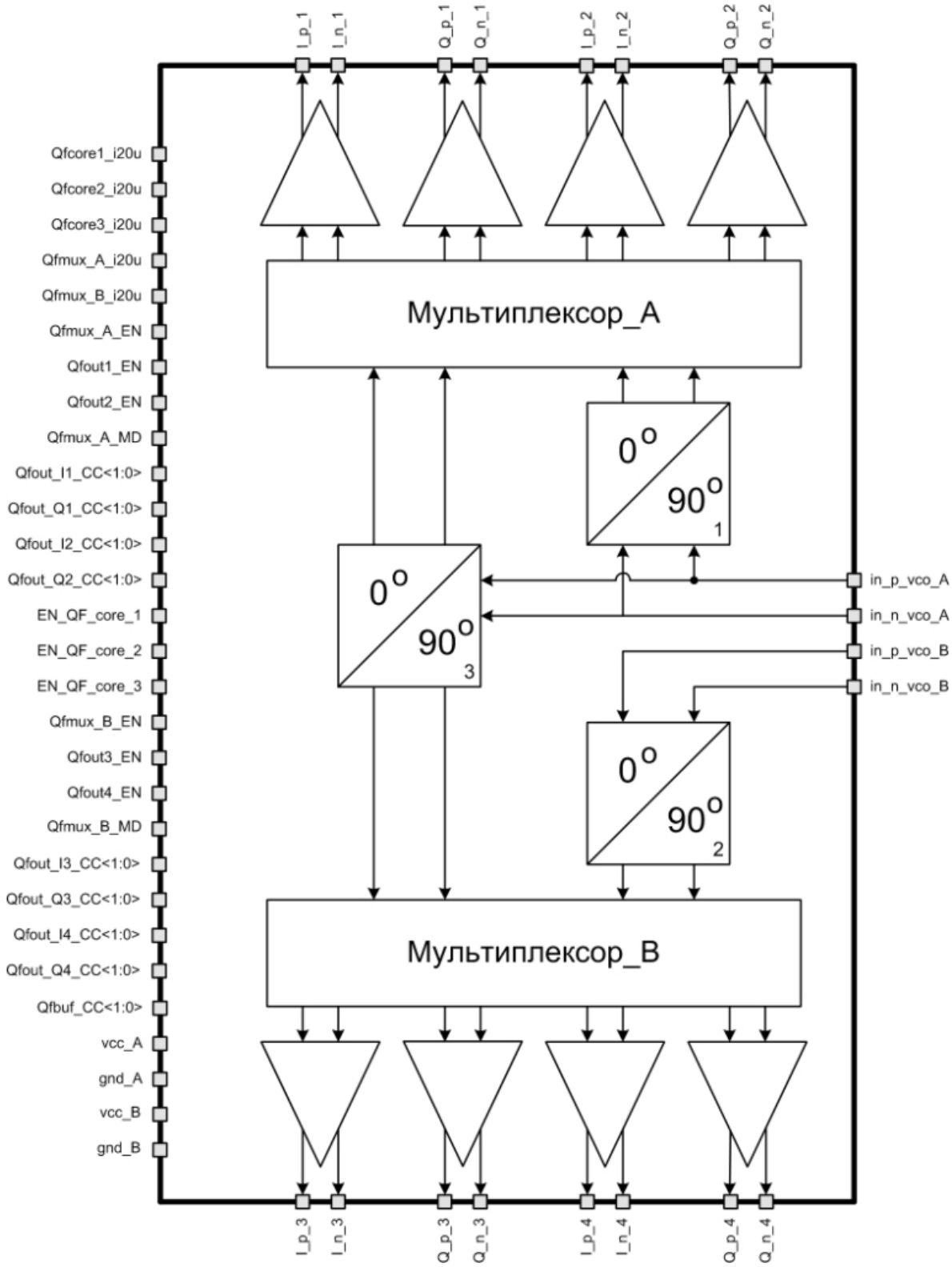

Figure 1: Quadrature former structure.

5 PIN DESCRIPTION

Name	Direction	Description
Qfmux_A_EN	I	Channel 1,2 output stage enable/disable
Qfout1_EN	I	Channel 1 output buffer enable/disable
Qfout2_EN	I	Channel 2 output buffer enable/disable
EN_QF_core_1	I	Channel 1,2 QF core enable/disable
EN_QF_core_2	I	Channel 3,4 QF core enable/disable
EN_QF_core_3	I	1,2,3,4 channel QF core enable/disable
Qfmux_B_EN	I	Channel 3,4 output stage enable/disable
Qfout3_EN	I	Channel 3 output buffer enable/disable
Qfout4_EN	I	Channel 4 output buffer enable/disable
Qfmux_A_MD	I	Channel 1,2 signal source selection
Qfmux_B_MD	I	Channel 3,4 signal source selection
in_p_vco_A	I	Signal A differential input
in_n_vco_A	I	
in_p_vco_B	I	Signal B differential input
in_n_vco_B	I	
I_p_1	O	Quadrature different output for channel 1
I_n_1	O	
Q_p_1	O	
Q_n_1	O	
I_p_2	O	Quadrature different output for channel 2
I_n_2	O	
Q_p_2	O	
Q_n_2	O	
I_p_3	O	Quadrature different output for channel 3
I_n_3	O	
Q_p_3	O	
Q_n_3	O	
I_p_4	O	Quadrature different output for channel 4
I_n_4	O	
Q_p_4	O	
Q_n_4	O	
Qfcore1_i20u	I	Reference current QF core 1 (20 µA)
Qfcore2_i20u	I	Reference current QF core 2 (20 µA)
Qfcore3_i20u	I	Reference current QF core 3 (20 µA)
Qfmux_A_i20u	I	Channel 1,2 stage reference current (20 µA)
Qfmux_B_i20u	I	Channel 3,4 stage reference current (20 µA)
Qfout_I1_CC<1:0>	I	Phase control for signal I channel 1
Qfout_Q1_CC<1:0>	I	Phase control for signal Q channel 1
Qfout_I2_CC<1:0>	I	Phase control for signal I channel 2
Qfout_Q2_CC<1:0>	I	Phase control for signal Q channel 2
Qfout_I3_CC<1:0>	I	Phase control for signal I channel 3
Qfout_Q3_CC<1:0>	I	Phase control for signal Q channel 3
Qfout_I4_CC<1:0>	I	Phase control for signal I channel 4

Table «Pin description» (continue)

Name	Direction	Description
Qfout_Q4_CC<1:0>	I	Phase control for signal Q channel 4
Qfbuf_CC<1:0>	I	Output buffers current consumption
vcc_A	IO	Supply voltage A
gnd_A	IO	Ground A
vcc_B	IO	Supply voltage B
gnd_B	IO	Ground B

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Blok dimension.

Dimension	Value	Unit
Height	730	µm
Width	460	µm

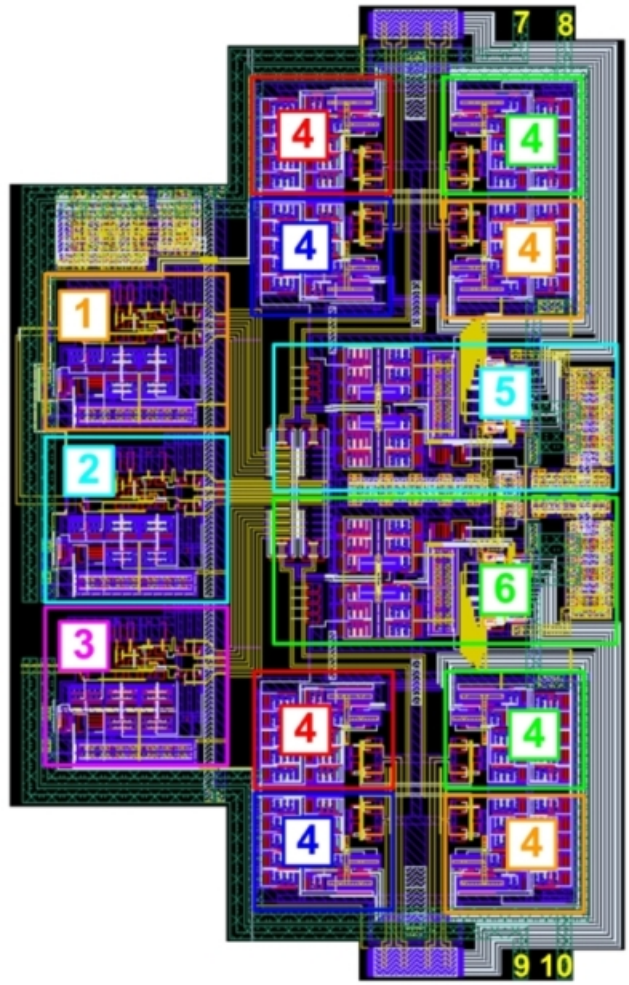

Figure 2: Device layout view

1. Quadrature 1
2. Quadrature 3
3. Quadrature 2
4. Output buffer
5. Multiplexer A
6. Multiplexer B
7. Power A
8. Ground A
9. Power B
10. Ground B

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ AMS035 BiCMOS 0.35 µm
Status _____ silicon proven
Area _____ 0.336mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.65 ÷ 3.15 V and T = -40 ÷ +85°C. Typical values are atV_{cc}= 2.7 V and T = +27°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	2.65	2.7	3.15	V
Operating temperature range	T	-	-40	+27	+85	°C
Input frequency range	F	-	2500	-	3800	MHz
Input differential signal voltage swing	$A_{in\ p\text{-}p}$	For input in_p_vco_A, in_n_vco_A, in_p_vco_B, in_n_vco_B.	400	-	-	mV
Differential output voltage swing, channel 1,2,3,4	$V_{dif\_p\_p}$	Gives for 50Ω and 150 fF differential load	460	600	620	mV
IQ phase error for any channel	φ_{errIQ}	-	-	-	±3	degree
Phase error between channels	φ_{err}	-	-	-	±1	degree
Phase adjustment range	φ	For output 1.6 GHz	-	±4.5	-	degree
Current consumption	I_{ccf}	All channels enabled (Qfbuf_CC<1:0> = “00”)	-	9	9.2	mA
Stand-by current	I_{stb}	-	-	0.01	0.1	µA
Input logic-level high	V_{IH}	For digital inputs	0.9 V_{cc}	-	V_{cc}	V
Input logic-level low	V_{IL}		-0.2	0	0.2	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

1. From version 1.0:
   - Section “Technical characteristics” (refer to page 6)