Power Management Unit

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- Input voltage range from 0.9V to 2.8V
- Adjustable output voltage
- External output capacitor required
- Embedded power on reset module
- Low quiescent current
- Supported foundries: TSMC, UMC, Global Foundries

2 APPLICATION

- Supply voltage sensitive circuits
- Battery-Powered equipment
- Power solutions

3 OVERVIEW

Power Management Unit (PMU) is designed to supply embedded integrated circuits with stable and precise internal voltage and currents. It integrates power switch element, LDO, Bangap and Power On Reset block.

PMU have controllable input voltage level and are complemented with VDD detectors to monitor the input voltage value. Two modes are available: full power mode and battery. If IO power voltage enable then LDO supply powered by 2.5V, if IO power voltage disable then LDO supply powered by battery power.

The voltage regulator consists of a differential amplifier which compares reference voltage with voltage from a feedback divider. It adjusts the impedance of a PMOS transistor for stabilization of output voltage at a set level.

PMU have Power On Reset block which generate logic level signal to control LDO power supply.

The block is fabricated on TSMC CMOS 65 nm technology.

4 STRUCTURE

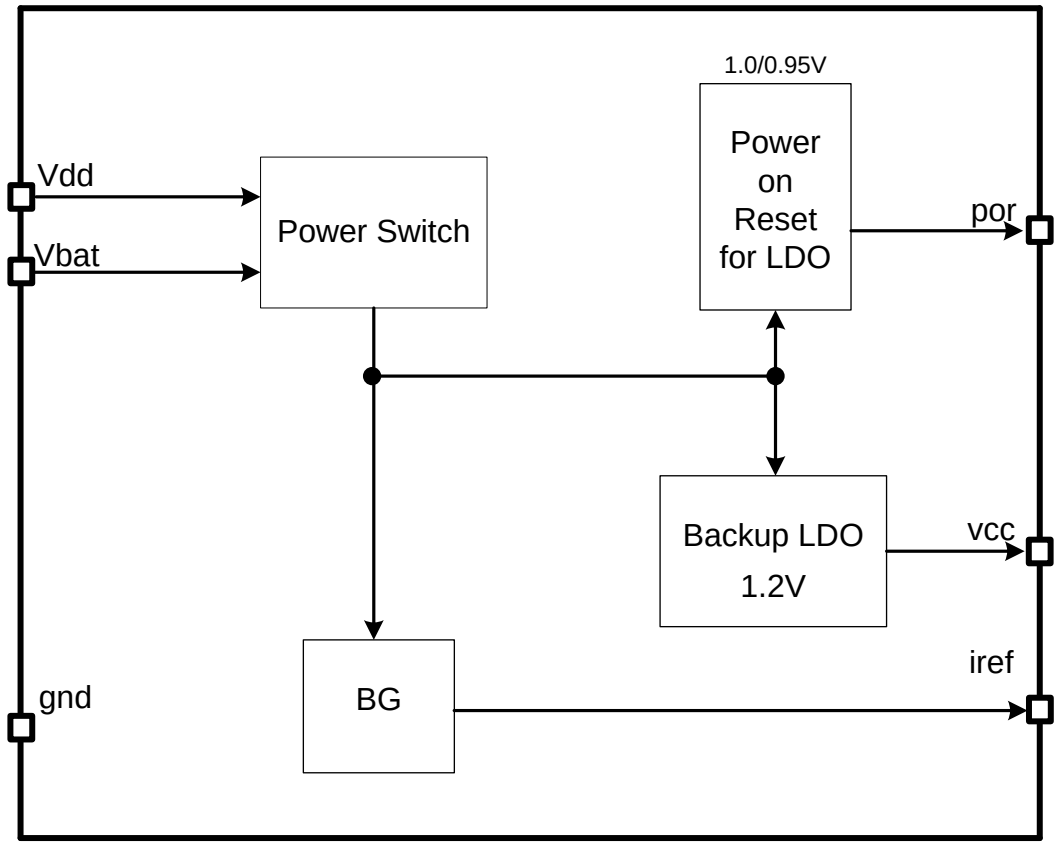

Figure 1: PMU structure

5 PINS DESCRIPTION

Name	Direction	Description
iref	O	Reference current
por	O	Power on reset output signal
vcc	O	LDO output supply voltage
vdd	P	Power supply (from 2.25 to 2.75 V)
vbat	P	Battery power supply (from 0.9 to 1.6 V)
gnd	P	Ground

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	235	um
Width	400	um

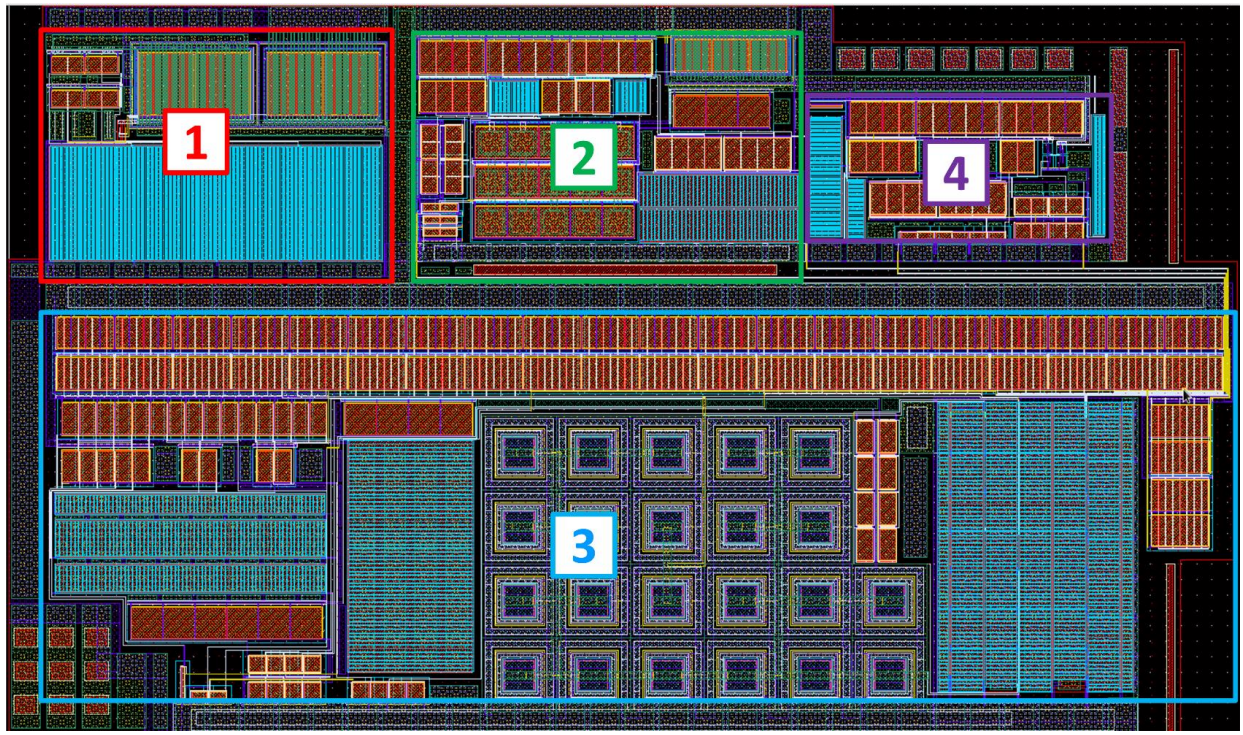

Figure 2: PMU layout structure

1. Power switch
2. LDO
3. Bandgap
4. Power on reset

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS 65nm
Status silicon proven
Area 0.094 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{bat} = 0.9 ÷ 1.6 V, V_{dd} = 2.25 ÷ 2.75 V and T = -40 ÷ +85°C. Typical values are at V_{dd}= 2.5V, T = +27°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Power supply	V_{dd}	-	2.25	2.5	2.75	V
Battery power supply	V_{bat}	$V_{bat} > V_{dd}$	0.9	-	1.6	V
Operating temperature range	T	-	-40	+27	+85	°C
Output voltage	V_{ldo}	Vdd=2.5V, external capacitor 1uF	1.19	1.201	1.22	V
Maximum load current	I_{out}	Vdd=2.5V	-	-	15	mA
Power on reset voltage	Vpwr_ldo	Vdd rising	-	1.001	-	V
		Vdd falling	-	0.952	-	
Reference current	I_{ref}	-	820	945	1103	nA
Supply current	I	$V_{dd} > V_{bat}$	-	22	-	µA
		$V_{bat} > V_{dd}$				
Battery Supply current	I_{bat}	$V_{dd} > V_{bat}$ and $V_{bat} < 1.5V$	-	-	0.4	uA

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation