# PVT Detector

# SPECIFICATION

## 1. FEATURES

- TSMC CMOS 40 nm
- High accuracy temperature and voltage measurements
- Process detector for all-voltage threshold MOS transistors
- Up to 8 remote temperature/voltage sensors
- Supported foundries: UMC, Global Foundries, AMS, SMIC, iHP, SilTerra

## 2. APPLICATIONS

- Die temperature monitoring
- Core voltage low battery indication
- Process deviation detection
- Pseudo static analog digitization
- System performance detection

## 3. OVERVIEW

PVT Detector is a unique solution intended to continuously monitor IC status at several on-die locations. It is able to detect manufacturing process deviation, perform voltage and die temperature measurement. PVT Detector (Figure 1) consists of PVT module (Figure 2), voltage/temperature sensor units and trimming units. PVT module is a calculation center that contains process detector units and is able to maintain up to 8 voltage/temperature sensor units.

# 4. STRUCTURE

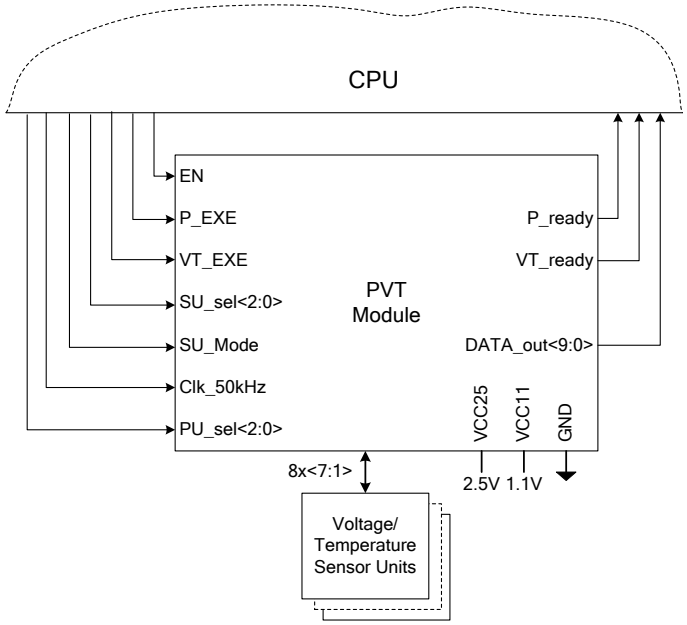


Figure 1: PVT Detector application schematic.

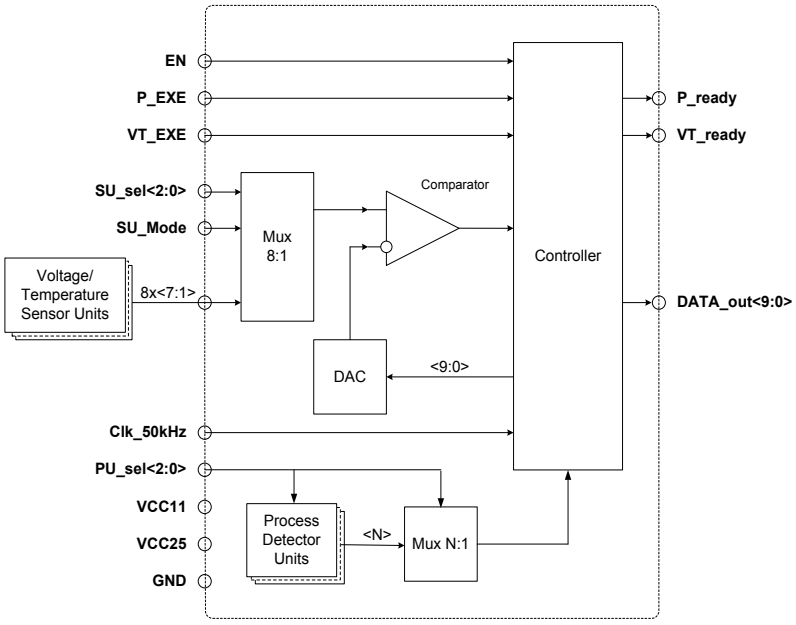


Figure 2: PVT Module block diagram.

# 5. PINS DESCRIPTION

Table 1: PVT module pin description.

| Name | Type | Direction | Description |
|---|---|---|---|
| EN | D (1.1V) | I | Enable PVT module |
| P_EXE | D (1.1V) | I | Process detection procedure execution |
| VT_EXE | D (1.1V) | I | Voltage/Temperature measurement procedure execution. |
| SU_Mode | D (1.1V) | I | Voltage or Temperature measurement mode selector |
| SU_sel<2:0> | D (1.1V) | I | Sensor Unit selector |
| PU_sel<2:0> | D (1.1V) | I | Process Detector selector |
| Clk_50kHz | D (1.1V) | I | External 50kHz clock |
| DATA_out<9:0> | D (1.1V) | O | Output data |
| P_ready | D (1.1V) | O | Process detection procedure ready flag |
| VT_ready | D (1.1V) | O | Voltage/temperature measurement procedure ready flag |
| sw<7:0> | D (1.1V) | I | On-sensor resistor divider enable, should be connected to the same-named port of corresponding Sensor Unit |
| V_pos<7:0> | A | I/O | Positive terminal for voltage measurement, should be connected to the same-named port of corresponding Sensor Unit |
| V_neg<7:0> | A | I/O | Negative terminal for voltage measurement, should be connected to the same-named port of corresponding Sensor Unit |
| Iref_in<7:0> | A | I/O | Reference current input terminal, should be connected to the same-named port of corresponding Sensor Unit |
| Iref_out<7:0> | A | I/O | Reference current output terminal, should be connected to the same-named port of corresponding Sensor Unit |
| pn_pos<7:0> | A | I/O | Positive terminal for temperature measurement, should be connected to the same-named port of corresponding Sensor Unit |
| pn_neg<7:0> | A | I/O | Negative terminal for temperature measurement, should be connected to the same-named port of corresponding Sensor Unit |
| VCC11 | A | P | Supply voltage 1.1 V |
| VCC25 | A | P | Supply voltage 2.5 V |
| GND | A | P | Ground |

Table 2: Sensor unit pin description.

| Name | Type | Direction | Description |
|---|---|---|---|
| sp_pos | A | P | Voltage measurement point |
| sp_neg | A | P | Local reference point. Should be connected to local ground of DUT |
| sw | D (1.1V) | I | Resistor divider enable |
| V_pos | A | I/O | Positive terminal for voltage measurement |
| V_neg | A | I/O | Negative terminal for voltage measurement |
| Iref_in | A | I/O | Reference current input terminal |
| Iref_out | A | I/O | Reference current output terminal |
| pn_pos | A | I/O | Positive terminal for temperature measurement |
| pn_neg | A | I/O | Negative terminal for temperature measurement |
| gnd | A | P | Local substrate contact |

# 6. LAYOUT DESCRIPTION

Table 3: PVT module block dimensions.

| Dimension | Value | Unit |
|---|---|---|
| Height | 418.1 | µm |
| Width | 206.5 | µm |

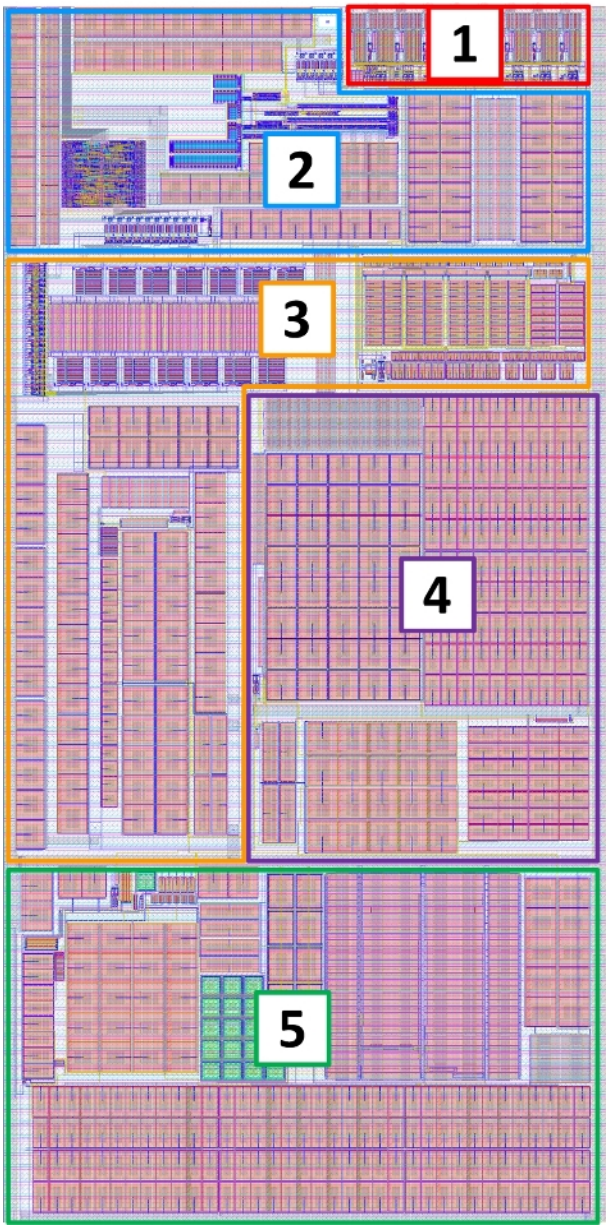


Figure 3: PVT module layout view.

1. MUX
2. Process detector
3. ADC
4. Reference current source
5. Bandgap

Table 4: Sensor unit block dimensions.

| Dimension | Value | Unit |
|---|---|---|
| Height | 28 | µm |
| Width | 14.4 | µm |

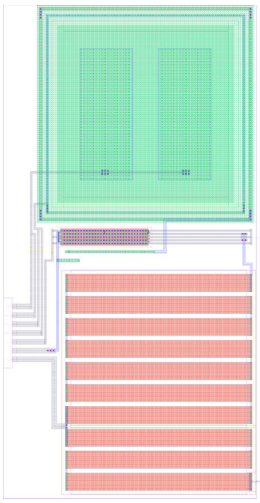

Figure 4: Sensor unit layout view.

# 7. ELECTRICAL CHARACTERISTICS

## 7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC CMOS 40 nm
Status _____ silicon proven
Area _____ 0.087 $mm^2$

## 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{cc25}$ = 2.4 V to 2.6 V, $V_{cc11}$ = 1.0 V to 1.2V, $T_j$ = -40 … +125°C. Typical values are at $V_{cc25}$ = 2.5 V, $V_{cc11}$ = 1.1 V, $T_j$ =+25°C, unless otherwise specified.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Core Supply Voltage | $V_{CC11}$ | | 1.0 | 1.1 | 1.2 | V |
| IO Supply Voltage | $V_{CC25}$ | | 2.4 | 2.5 | 2.6 | V |
| Operating Temperature Range | $T_j$ | | -40 | +25 | +125 | °C |
| Current Consumption | $I_{CC11}$ | | - | 250 | 400 | uA |
| | $I_{CC25}$ | | - | 390 | 500 | |
| Current Consumption in standby mode | $I_{STBY11}$ | @ $V_{CC11}$ | - | 2.5 | 55 | uA |
| | $I_{STBY25}$ | @ $V_{CC25}$ | - | - | 2 | uA |
| Digital Input-Logic High | $V_{IH}$ | | * | - | * | V |
| Digital Input-Logic Low | $V_{IL}$ | | * | - | * | |
| Digital Output-Logic High | $V_{OH}$ | | * | - | * | |
| Digital Output-Logic Low | $V_{OL}$ | | * | - | * | |
| Voltage Measurement Range | $V_{MR}$ | | 0.8 | - | 1.35 | V |
| Temperature Measurement Range | $T_{MR}$ | | -40 | - | 125 | °C |
| Temperature measurement accuracy | $A_T$ | with trimming | - | - | ±2 | °C |
| | | w/o trimming | - | - | ±5 | |
| Voltage measurement accuracy | $A_V$ | with trimming | - | - | ±2 | % |
| | | w/o trimming | - | - | ±5 | |
| Output DATA resolution | K | | - | 10 | - | bit |
| Clock frequency | $f_{CLK}$ | | 40 | 50 | 60 | kHz |

*Value is defined by TSMC N40LP standard cell library tcbn40lpbwp

# 8. DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation