

# Tunable oscillator of reference frequency

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## SPECIFICATION

### 1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Operation at the 1<sup>st</sup> or the 3<sup>rd</sup> harmonic of a quartz resonator
- The 2<sup>nd</sup> or the 3<sup>rd</sup> output harmonic selection
- Oscillator frequency shift keying signal
- External frequency oscillator operation in a buffer mode
- Low current consumption
- High temperature stability using temperature-compensated resonator
- Low frequency time response
- Small area
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

### 2 APPLICATION

- Frequency multiplier
- Reference signal former
- PLL frequency synthesizer
- Transmitters

### 3 OVERVIEW

Reference oscillator is used to generate reference frequency and can work at the 1<sup>st</sup> or the 3<sup>rd</sup> harmonic of quartz crystal resonator. Operating frequency is defined by external quartz resonator and external component values. Output peak-to-peak limitation system is used to reduce current consumption. Commutable capacitors are used to change carrier frequency that allows generating a frequency shift keying signal in a case of application in a transmitter. Output resonant circuit is used to select the 2<sup>nd</sup> or 3<sup>rd</sup> harmonic (see section 7.3).

The block is fabricated iHP SiGe BiCMOS 0.25 um technology.

## 4 STRUCTURE

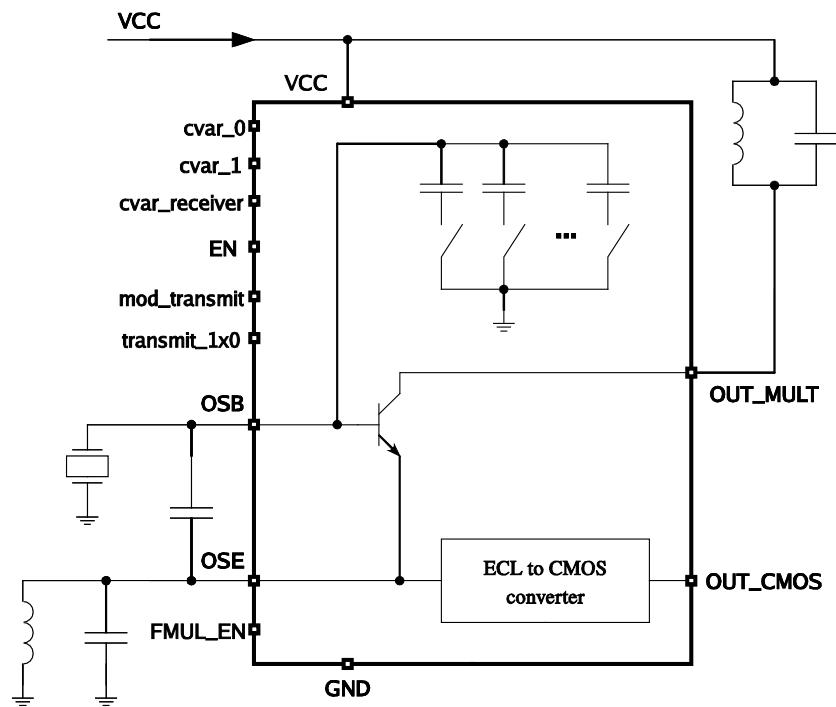


Figure 1: Structure of the device with the harmonic selection at the oscillator output.

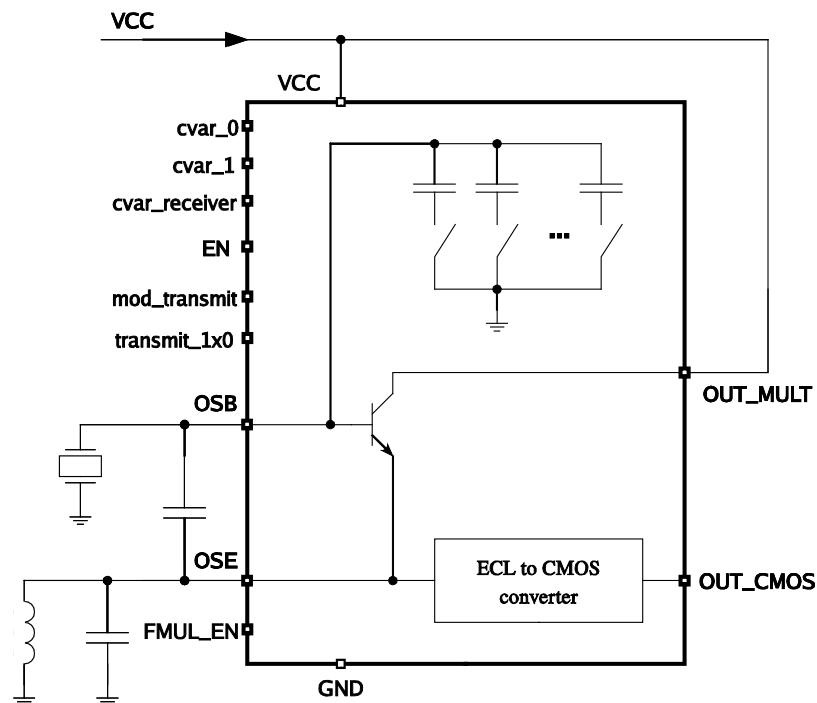


Figure 1: Structure of the device without the harmonic selection at the oscillator output.

## 5 PIN DESCRIPTION

Name	Direction	Description
mod_transmit	I	Trimming capacitors adjustment enable
transmit_1x0	I	Modulation signal input
FMUL_EN	I	Trimming capacitors disable
cvar_0	I	Frequency-shift keying mode selection
cvar_1	I	
cvar_receiver	I	
EN	I	Enable/disable
OUT_MULT	O	Analog output
OUT_CMOS	O	CMOS output
OSB	IO	Analog output for quartz resonator connection
OSE	IO	Oscillator core collector output
GND	IO	Ground
VCC	IO	Supply voltage

## 6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

**Table 1:** Block dimensions.

Dimension	Value	Unit
Height	520.41	um
Width	305.52	um

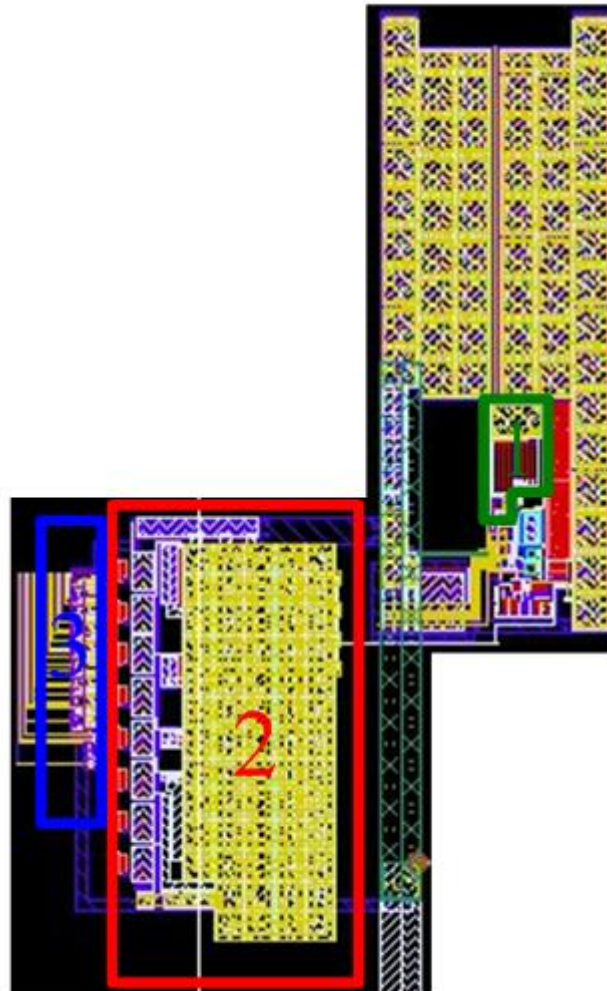


Figure 3: Device layout view.

1. ECL to CMOS converter
2. Trimming capacitors
3. Trimming capacitors adjustment

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ iHP SiGe BiCMOS 0.25 um  
 Status \_\_\_\_\_ silicon proven  
 Area \_\_\_\_\_ 0.065 mm<sup>2</sup>

### 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{cc} = 1.8 \div 2.3$  V and  $T_a = -45 \div +85$ °C. Typical values are at  $V_{cc} = 2.2$  V,  $T_a = +27$  °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	$V_{cc}$	-	1.8	2.2	2.3	V
Operating temperature range	$T_a$	-	-45	27	85	°C
Output frequency	$F_{out}$	Depends on connected crystal; 1 <sup>st</sup> harmonic of oscillator	18	26	90	MHz
Peak-to-peak input voltage	$A_{XTALL}$	-	-	1.2	-	V
Peak-to-peak output voltage	$A_{out\_XTALL}$	-	350	550	-	mV
Peak-to-peak CMOS input voltage	$A_{out\_XTALLcmos}$	-	1.8	2.2	2.3	V
Frequency tuning range	$\Delta F$	-	1	1.45	2.1	kHz
Frequency time response	$t_{stab}$	-	-	1.4	2	ms
Current consumption in an active mode	$I_{cc}$	-	135	160	260	uA
Current consumption in a standby mode	$I_{stb}$	-	-	1.5	5	nA
Input logic-high level	$V_{IH}$	For digital inputs	$0.7V_{cc}$	-	$V_{cc}+0.25$	V
Input logic-low level	$V_{IL}$		-0.25	-	0.3	V

### 7.3 FREQUENCY OPERATING MODE

	Extracted harmonic of the output signal		
	1 <sup>st</sup> oscillator harmonic	2 <sup>nd</sup> oscillator harmonic	3 <sup>rd</sup> oscillator harmonic
1 <sup>st</sup> resonator harmonic	19...30 MHz	38...60 MHz	57...90 MHz
3 <sup>rd</sup> resonator harmonic	57...90 MHz	114...180 MHz	171...270 MHz
In a buffer mode	19...90 MHz	38...180 MHz	57...270 MHz

## 8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation