Controller CAN

SPECIFICATION

1 FEATURES

- SMIC CMOS 180 nm.
- Multiple Master Devices architecture.
- Message priority determined with Identifier (11 bits or extended 29 bits).
- Bitwise arbitration algorithm that can transmit messages without errors in the case of multiple CAN nodes simultaneous transmission.
- Programmable bit rate.
- Statistical error control and the interfering nodes disconnection from bus.
- VHDL RTL compatible with Synopsys, Autologic, etc. synthesizing tools.
- Synthesis to FPGA option.

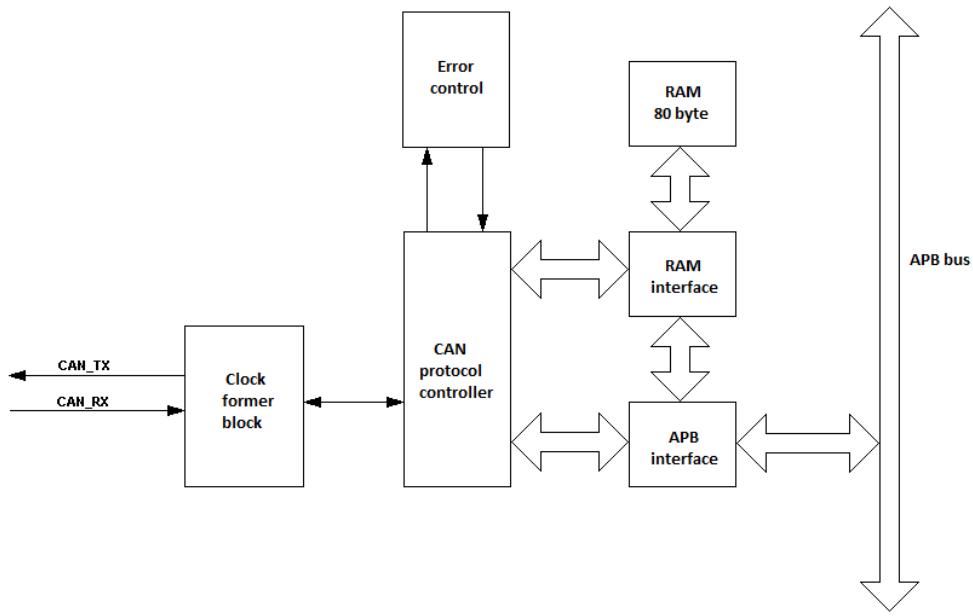
2 APPLLICATION

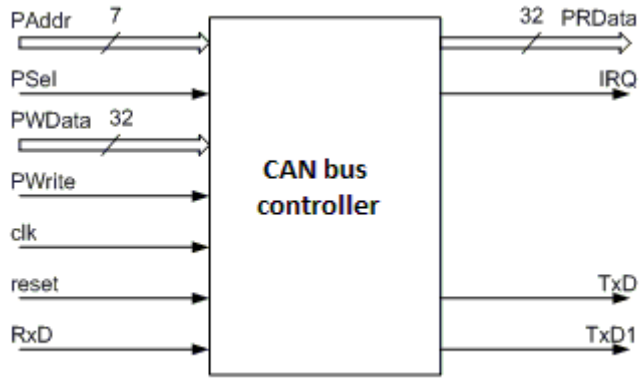
- ASIC

3 OVERVIEW

CAN (Controller Area Network) performs data exchange under specification CAN 2.0V. The controller connected to 32-bit data bus APB and his outputs CAN_TX and CAN_RX are inputs for external CAN-transceiver.
Controller realized in SMIC CMOS 180 nm technology.

4 STRUCTURE





5 PIN DESCRIPTION

Name	Direction	Description
System interface		
PAddr[6:0]	I	APB address
PSel	I	APB selection
PWData[31:0]	I	Data to APB bus
PWrite	I	APB write signal
clk	I	APB clock signal
reset	I	Reset signal
IRQ	O	Interruption request output
PRData[31:0]	O	Data from APB bus
CAN-transceiver side interface		
RxD	I	Receiver input
TxD	O	Transmitter output
TxD1	O	Transmitter auxiliary output

6 DELIVERABLES

IP contents include:

- RTL Code (VHDL 1076 1993)
- Behavioral model for testing (VHDL 1076 1993)
- Script example for synthesis in Synopsys
- Synopsys timing constraints example
- Synopsys CBA library netlist (VHDL 1076 1993) example