Corrector ADC

SPECIFICATION

1 FEATURES

- SMIC EEPROM CMOS 90 nm
- Control ADC offset
- Control amplitude imbalances
- Control phase imbalance
- Estimates average signal power
- FPGA and ASIC implementations available
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATIONS

- DSP systems
- Digital receivers

3 OVERVIEW

This IP provides a DC offset removal at the ADC output, the channel amplitude and phase imbalances cancelation. The corrector is fully parameterized allows you to quickly control the speed of convergence of the each chain correction. The block diagram contains the average signal power estimator required for the subsequent removal amplitude imbalance of the channels. The synchronous sampling circuits are used to eliminate the phase error between the reception channels for the automatic gain control and diagnostics. The corrector incorporates four feedback loops, each of which is responsible for adjusting individual parameters of the complex signal from the ADC. Upon opening of the loops, the unit operates in the transmission mode to output without change.

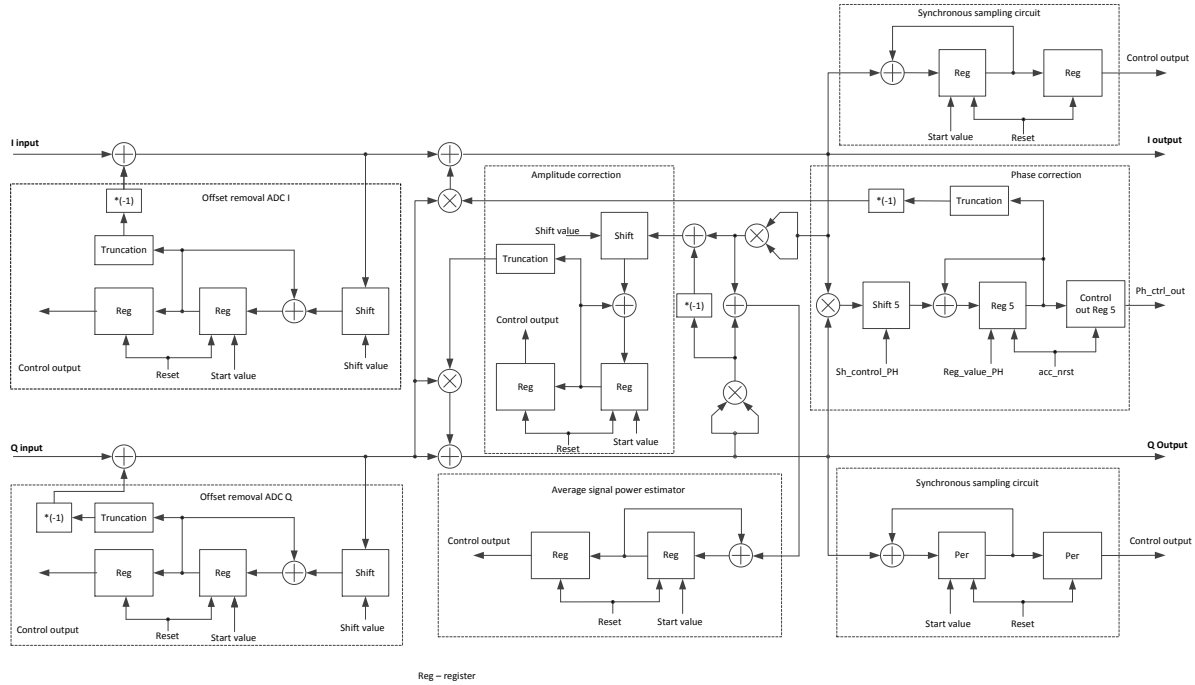

Figure 1: Block-diagram of the corrector ADC

4 PIN DESCRIPTION

Name	Direction	Bits	Description
Clock	I	1	Clock signal
Set	I	1	Asynchronous reset (low - active)
enclk	I	1	Enable Clock
acc_nrst	I	1	Clock signal for latching a current data from the correction accumulators to corresponding outputs monitoring registers
Set_reg	I	1	Load pulse for all start values of the all registers-accumulators (all registers load simultaneously).
I_in	I	16	Input data (I-channel)
Q_in	I	16	Input data (Q-channel)
Reg_Value_sI_in	I	16	Start value of the accumulator (16 high bits) of the synchronous sampling circuit (I-channel)
Reg_Value_sQ_in	I	16	Start value of the accumulator (16 high bits) of the synchronous sampling circuit (Q-channel)
Reg_Value_zI_in	I	16	Start value of the accumulator (16 high bits) of the DC offset removal unit (I-channel)
Reg_Value_zQ_in	I	16	Start value of the accumulator (16 high bits) of the DC offset removal unit (Q-channel)
Reg_Value_AM_in	I	16	Start value of the accumulator (16 high bits) of the amplitude correction unit
Reg_Value_PH_in	I	16	Start value of the accumulator (16 high bits) of the phase correction unit
Reg_Value_Pow_in	I	16	Start value of the accumulator (16 high bits) of the average power estimator
Sh_control_z	I	6	Speed of convergence control code for DC offset removal units, master bit is responsible for the opening of the loop (high – closed loop)
Sh_control_AM	I	6	Speed of convergence control code for amplitude correction, master bit is responsible for the opening of the loop (high – closed loop)
Sh_control_PH	I	6	Speed of convergence control code for phase correction, master bit is responsible for the opening of the loop (high – closed loop)
Sinhr_Q_out	O	32	Value of the accumulator of the synchronous sampling circuit (Q-channel)
Sinhr_I_out	O	32	Value of the accumulator of the synchronous sampling circuit (I-channel)
Pow_ctrl_out	O	32	Value of the accumulator of the average power estimator
Ph_ctrl_out	O	32	Value of the accumulator of the phase correction unit

Table "pin description" (continue)

Name	Direction	Bits	Description
Am_ctrl_out	O	32	Value of the accumulator of the amplitude correction unit
Zero_ctrl_outQ	O	32	Value of accumulator of the DC offset removal unit (Q-channel)
Zero_ctrl_outI	O	32	Value of accumulator of the DC offset removal unit (I-channel)
I_out	O	16	Output data (I-channel)
Q_out	O	16	Output data (Q-channel)

5 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions.

Dimensions	Value	Unit
Height	400	um
Width	200	um

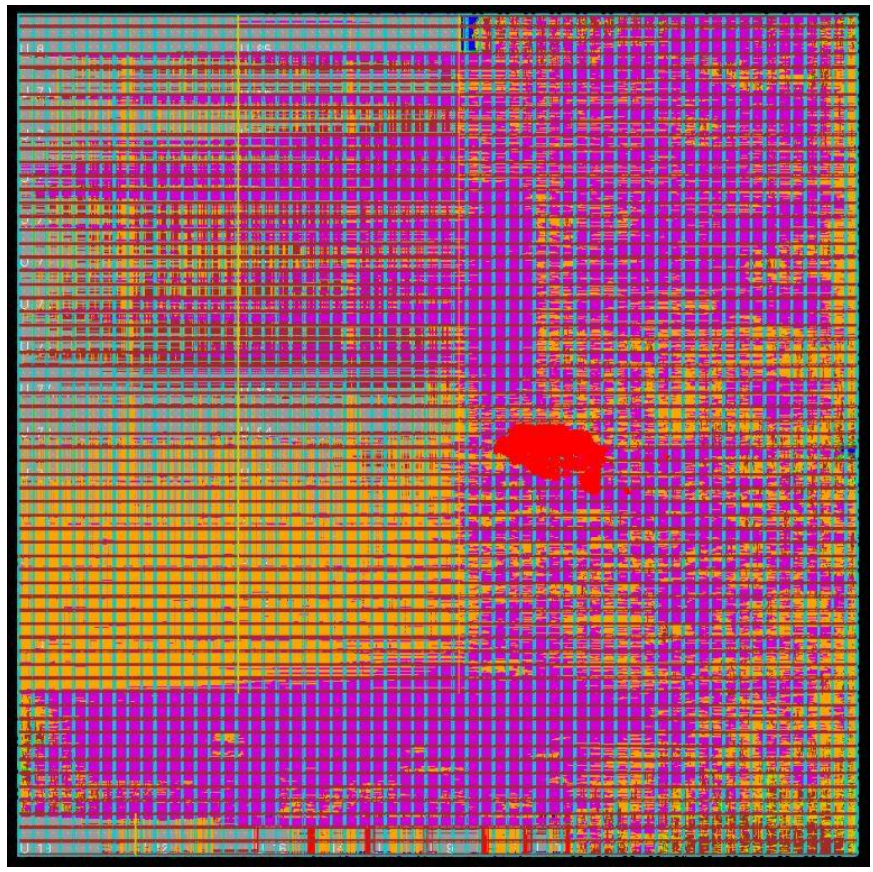

Figure 2: Corrector ADC layout view.

6 OPERATING CHARACTERISTICS

6.1 TECHNIKAL CHARACTERISTICS

Technology SMIC EEPROM CMOS 90 nm
Status silicon proved
Max frequency for FPGA 59.2 MHz
Triggers 882
Amplitude correction range 50%
Phase correction range 5 degree
Area 0.08 mm^2

6.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd}=0.9÷1.1 V and T_j =-60÷+125°C, unless otherwise specified; typical values are at V_{dd}=1.0 V and T_j = +27°C.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Operating temperature range	T_j	-	-60	27	125	°C
Supply voltage	V_{dd}	-	0.9	1.0	1.1	V
Max amplitude input signal	A_{IN}	-	1.020	1.024	1.030	V
Input high level	V_{IH}	For digital inputs	0.7	-	-	V
Input low level	V_{IL}		-	-	0.3	V

7 DELIVERABLES

IP contents:

- xHDL behavior model
- Documentation